Design and Implementation of High Frequency Isolated AC-DC Converter for Switched Mode Power Supplies

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***Abstract*—In this paper the design and implementation of DC-DC converter based SMPS for a telecommunication system is presented. A high frequency transformer is used to provide the galvanic isolation between the input and output. A complete design methodology of high frequency transformer used for full-bridge buck derived topology is presented. The operating modes, analysis, and design considerations are explained for the proposed converter. Simulation and experimental results are also presented to demonstrate the performance of the proposed converter.**

Keywords—High frequency isolation; Single-stage converter; Power factor correction (PFC); Full-bridge buck converter; SMPS

I. INTRODUCTION

The use of three-phase ac-dc converters for telecommunication power supply system [1] have led to an increased harmonic content being injected into the utility mains and low power factor, both caused by the non-linear load behavior of conventional diode-rectifiers.

Telecommunication power supplies have to confirm to low THD input ac mains current and high PF as per IEC 61000-3-2 [2] and IEEE 519-1992 standards [3]. The advantage of reducing the stress on the devices by single stage PFC and soft switching techniques are discussed in the literatures [4] & [5]. A three-phase converter using single-phase modular rectifier topology has the merits of simple control. They are becoming popular for low-voltage or medium-power supply applications [6]-[8].

In this paper, a high frequency (HF) isolated ac-dc converter with input power factor almost unity is presented. The single-phase module is operated from 230V, 50Hz input to give regulated output of 325V with a switching frequency of 35 kHz. The circuit configuration, design and implementation of the converter using digital controller is presented. Finally, simulation and experimental results are presented to demonstrate its satisfactory performance.

II. PROPOSED CONVERTER TOPOLOGY FOR SMPS

Fig. 1 shows the switched mode power supply topology for telecom power supply applications with the full-bridge buck dc-dc converter incorporating PFC.

A. Operation Principle of the DC-DC Converter

For three phase operation the three set of single phase converter can be used. Fig. 2a shows the one single-phase converter module which is used for the steady state analysis and design purpose. It has a dc voltage source from the diode-bridge rectifier with a series inductor feeding to the full-bridge dc-dc converter.

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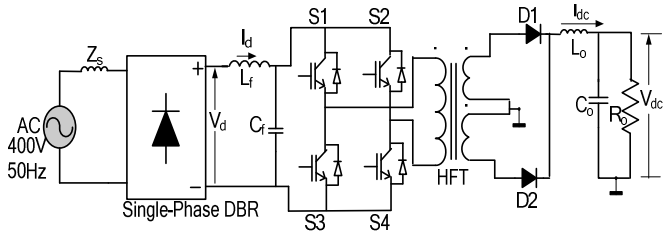

Fig. 1 Schematic diagram of the HF isolated dc-dc converter

The full-bridge buck converter has four IGBT switches (S1, S2, S3 and S4) and it is feeding to the high frequency transformer for providing galvanic isolation. The switches are ON alternatively in each half of PWM period with the controlled width of pulse decided by duty ratio from the PI controller. The operation of the converter for one half-cycle using the equivalent circuits is explained in the following section.

B. Analysis and Design of the DC-DC Converter

In this section, the steady state analysis of the proposed converter is carried out to obtain the required design equations and the parameters of the converter.

For the design and analysis of the full-bridge converter, it is considered that all the switches are ideal. The full-bridge dc-dc converter has two intervals of operation in each half cycle. To operate at CCM, the current should not touch zero at the end of interval 1. Fig. 2 shows the basic circuits of a full-bridge buck dc-dc converter for the two intervals. In interval 1, S1 and S4 are on. In interval 2 all the four switches are off. The two interval of operation are explained in detail as below.

Interval 1: T_o<t<DT_s

In this interval, two diagonal switches S1 and S4 are ON and delivering energy to the load through a high frequency transformer and two diodes. For this purpose the circuit model as shown in Fig. 2b is considered.

$$V_p = V_d \tag{1}$$

$$V_{s1} = (N_{s1}/N_p)V_d ; V_{s2} = (N_{s2}/N_p)V_d \tag{2}$$

The voltage across the output inductor L_o, V_L is as,

$$V_L = (N_{s1}/N_p)V_d - V_{dc} \tag{3}$$

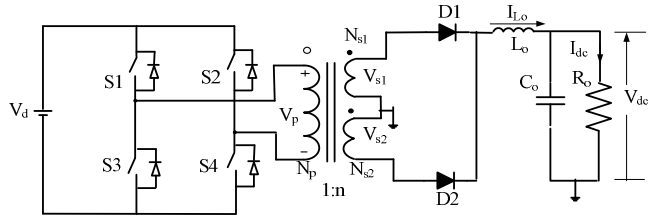

Fig. 2a

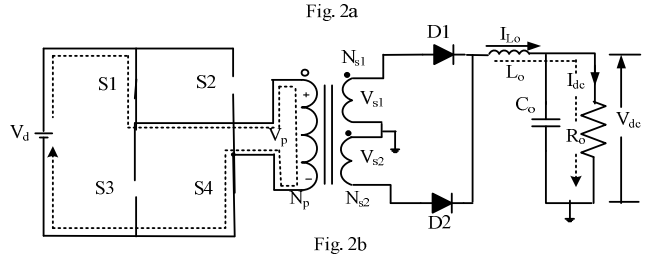

Fig. 2b

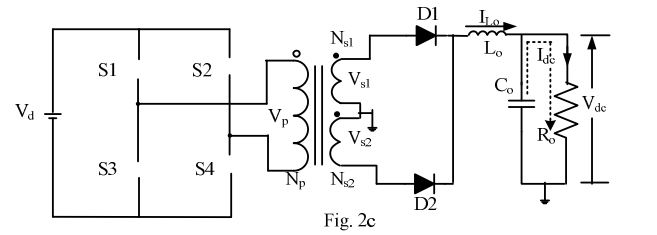

Fig. 2c

Fig. 2a Schematic diagram for analysis single-phase module full-bridge boost converter (b) Interval 1 (c) Interval 2

where, V_p is the voltage across the primary winding of the high frequency transformer. V_{s1} and V_{s2} are the voltages across the secondary windings of the high frequency transformer. V_d is the input dc voltage for the full-bridge dc-dc converter. V_L is the voltage across the output inductor L_o. V_{dc} is the dc output voltage across the load. N_p, N_{s1} and N_{s2} are the number of turns of the primary and secondary windings of the high frequency transformer.

The rate of rise of the inductor current i_{Lo} is given as,

$$\frac{di_{Lo}}{dt} = \frac{V_L}{L_o} = \frac{(N_{s1}/N_p)V_d - V_{dc}}{L_o} \quad (4)$$

The change in the inductor current during the on period is as,

$$(\Delta i_L)_{ON} = \frac{(n V_d - V_{dc})}{L_o}(\Delta t)_{ON} \quad (5)$$

$$(\Delta i_L)_{ON} = \frac{(n V_d - V_{dc})}{L_o} D T_S \quad (6)$$

where, $n=(N_{s1}/N_p) = (N_{s2}/N_p)$ and duty cycle, $D=(2T_{ON}/T_s)$.

Interval 2: $DT_s < t < T_s/2$

In this interval all switches are off during the period $DT_s < t < (T_s/2)$ and the load current flows through the diodes. The equivalent circuit can be drawn as shown in Fig. 2c. The rate of change of output inductor current is

$$\frac{di_{Lo}}{dt} = \frac{-V_{dc}}{L_o} \quad (7)$$

The change in inductor current during the off period is as,

$$(\Delta i_L)_{OFF} = \frac{-V_{dc}}{L_o}(\Delta t)_{OFF} \quad (8)$$

$$T_{OFF} = \frac{T_s}{2} - T_{ON} = 0.5T_s - T_{ON} \quad (9)$$

$$T_{OFF} = (0.5 - D)T_s \quad (10)$$

Substituting equation (10) in equation (8), the change in the inductor current is obtained as,

$$(\Delta i_L)_{OFF} = \frac{-V_{dc}}{L_o}(0.5 - D)T_S \quad (11)$$

Under steady state condition, the change in the inductor current is zero over a half period $T_s/2$.

$$(\Delta i_L)_{ON} + (\Delta i_L)_{OFF} = 0 \quad (12)$$

Substituting equation (6) and (11) in equation (12) as,

$$\frac{(n V_d - V_{dc})D T_S}{L_o} + \frac{-(0.5 - D)V_{dc}T_S}{L_o} = 0 \quad (13)$$

On solving, eqn. (13) results in

$$V_{dc} = 2n \; D \; V_d \quad (14)$$

From equation (14) it is known that the output voltage can be varied by adjusting the duty ratio of the switch (D) and the high frequency transformer turns ratio (n). During the period the inductor current increases linearly as,

$$(\Delta i_L)_{ON} = \frac{(n V_d - V_{dc})}{L_o}(\Delta t)_{ON} \quad (15)$$

$$I_{Lo,max} - I_{Lo,min} = \frac{(n V_d - V_{dc})}{L_o} T_{ON} \quad (16)$$

$$(\Delta i_L)_{ripple} = \frac{(n V_d - V_{dc})}{L_o} T_{ON} \quad (17)$$

Similarly, during the period when all the switches are off, the current in the inductor reduces as per eqn. (11).

$$I_{Lo,min} - I_{Lo,max} = \frac{-V_{dc}}{L_o}(0.5 - D)T_S \quad (18)$$

$$I_{Lo,max} - I_{Lo,min} = \frac{V_{dc}}{L_o}(0.5 - D)T_S \quad (19)$$

$$(\Delta i_L)_{ripple} = \frac{V_{dc}}{L_o}(0.5 - D)T_S \quad (20)$$

Therefore the value of the inductor is given as,

$$L_o = \frac{(0.5 - D)V_{dc}T_S}{(\Delta i_L)_{ripple}} \quad (21)$$

Fig. 3 shows the output inductor current and amplified output voltage typical waveforms in CCM. The ripple voltage across the filter can be calculated as,

$$\Delta Q = C_o \Delta V_o \quad (22)$$

where, ΔV_o is the output ripple voltage. This ΔV_o can be considered as,

$$\Delta V_o = \frac{\Delta Q}{C_o} \quad (23)$$

The change in the charge ΔQ can be calculated from the area of the triangle representing the positive current as shown in Fig. 3 and expressed as,

$$\Delta Q = \frac{1}{2} * \frac{T_s}{4} * \frac{\Delta i_L}{2} \quad (24)$$

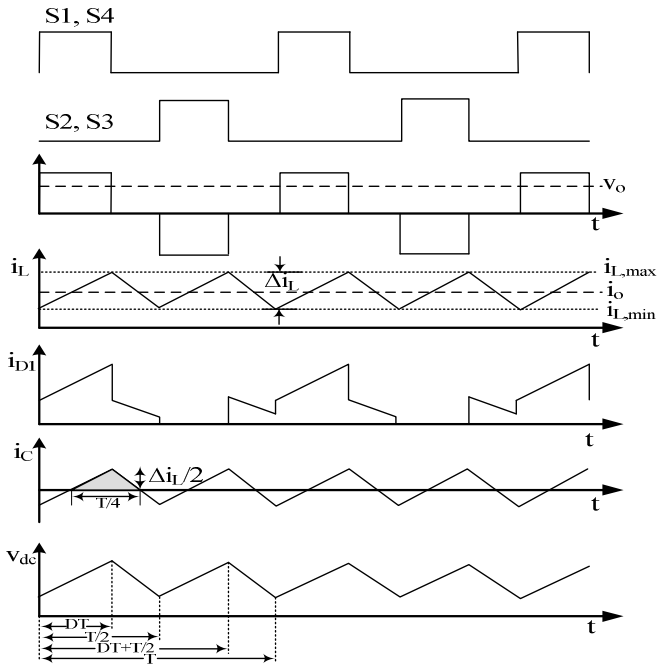

Fig. 3 Characteristic waveforms of the full-bridge buck dc-dc converter

The boundary between the CCM and DCM, by definition the inductor current i_L reduces to zero at the end of the off period. At this boundary the average inductor current is,

$$I_L = I_o = \frac{\Delta i_L}{2} \tag{25}$$

Substituting equation (25) in equation (24), the change in the capacitor charge is given by,

$$\Delta Q = \frac{1}{2} * \frac{T_s}{4} * I_L \tag{26}$$

Substituting equation (26) in eqn. (23), the output voltage ripple is given as,

$$\Delta V_o = \frac{T_s I_L}{8 C_o} \tag{27}$$

Therefore, the output capacitor can be found from the ripple voltage as,

$$C_o = \frac{T_s I_L}{8 (\Delta V_o)_{ripple}} \tag{28}$$

Equation (28) is the boundary between CCM and DCM.

The magnitude of output voltage ripple is reduced by properly designing the converter components. The basic equation for the current flowing through the inductor is, $V = L_o (\Delta I_o/\Delta T)$, on rearranging

$$L_o = V (\Delta I_o/\Delta T)$$

To compute the value of inductance

$$L_o = \{(0.5\text{-}D) V_{dc} T_s /(\Delta i_L)_{ripple}\} \tag{29}$$

where the duty ratio 'D' is considered to be 0.45,output dc voltage V_{dc}=60V, Load current I_{dc}=200A; switching frequency f_s=35kHz, T_s=29e-6 sec; ripple current is 2% of the load current, $(\Delta i_L)_{ripple}$=4A. Substituting these values in equation (29) the value of the inductor is found to be;

$$L_o = [\{(0.5\text{-}0.45) (60) (29) (10e^{-6})\} / 4] = 21.75\mu H$$

Approximating the calculated value, an inductor of L_o =20μH is chosen. Inductors with EE shape 65/39 on ferrite core; two turns with a 20 SWG wire is chosen for the hardware implementation. For obtaining the value of capacitor the following values are used; ΔV_o=1% of the output voltage V_{dc} =60V, therefore ΔV_o = 0.6V .The value of the output capacitor C from equation (30) is as,

$$C_o = (D T_s I_{dc} /\Delta V_o) \tag{30}$$

$$= [\{(0.5) (29)(10e^{-6})(200)\}/0.6] = 4833\mu F$$

An electrolytic capacitor of 7x680 μF, 100V capacitance which easily meets the minimum requirements is chosen for the hardware.

C. Design of High Frequency Transformer

The design of high frequency transformer used for full-bridge buck derived topology is presented in this section. The purpose of a high frequency transformer in SMPS is to transfer power efficiently and instantaneously from an electric source to an external load. In doing so, the high frequency transformer also provides important additional capabilities:

(i) The primary to secondary turn's ratio can be established efficiently to accommodate widely different input and output voltage levels. (ii) Separate primary and secondary windings facilitate high voltage input/output isolation, especially important for safety applications.

The steps for designing a high frequency transformer for switch mode power supplies are outlined below. The approach presented here is logical and a step by step procedure is illustrated by considering full-bridge buck dc-dc converter as an example.

Step 1: Define the switched mode power supply parameters pertaining to the high frequency transformer design. Circuit topology: full-bridge buck dc-dc converter Power Output, P_o= 2kW; Transformer switching frequency f_s=35kHz; Input voltage, V_{in}= 560V; Output voltage, V_o= 20V, Output current I_o= 100A

Step 2: Define the absolute duty cycle limit and nominal D_{max} at input voltage $V_{in\text{-}D}$. D_{max}=0.5; D_{min}=0.45

Nominal input voltage $V_{in\text{-}D}= V_{in}D_{max}$= (560) (0.5) = 280V

Step 3: Calculate the nominal output voltage by including the diode voltage drops. As there are two rectifier diodes at the secondary side, a voltage drop of 1.6V is added to the output voltage. Nominal output voltage $V_{o\text{-}D}$ = 20+1.6=21.6V

Step 4: Calculate the turn's ratio 'n' of the high frequency transformer.

n= $(V_{in\text{-}D} /V_{o\text{-}D})$ = (280/21.6) = 12.96 approximated to 13 turns across each secondary winding. The possible choices of turn's ratio are 26:1, 210:8.

Since, the high frequency transformer is followed by centre-tapped diode rectification it has one primary and two secondary windings. Primary winding of 210 turns and secondary

winding of 8 turns, each secondary winding of 4 turns is the possible choice of turns chosen for the design of high frequency transformer.

Step 5: Calculate the current flowing through each winding of the high frequency transformer.

Nominal output current $I_{o\text{-}D}= I_oD_{max}= (100)\ (0.5) = 50A$

Nominal input current, $I_{in\text{-}D}= (I_{o\text{-}D}/n) = (50/13) = 3.84$

Therefore the primary current flowing through the high frequency transformer is 4A.

Step 6: The final step is the core material, shape and size selection for the high frequency transformer. The core material is selected appropriate for the desired high frequency transformer. With power ferrites, higher frequency materials have higher resistivity, hence lower eddy current losses. It is the best choice in transformer applications except for mechanical ruggedness.

It usually needs some guidance in making an initial estimate of the core size appropriate for the application of switched mode power supply requirements. One widely used method, with many variations, is based on the core area product A_p, obtained by multiplying the effective core magnetic cross-section area A_e by the window area A_w available for the winding. The following formula provides a simple indication of the area product required:

$$A_p = A_wA_e = \left(\frac{P_o}{K_u\ \Delta B\ f_S}\right)^{4/3} \text{cm}^4 \qquad (31)$$

where, K_u is the core utilization factor. It is assumed as 0.017 for full-bridge and half-bridge dc-dc converter. ΔB is the flux density. A value can be chosen in between 0.2-0.35 Tesla for limiting the core saturation. It is assumed as 0.25 Tesla. Therefore, the core area product is

$$= \left\{\frac{12 \times 10^3}{(0.017)(0.25)(35 \times 10^3)}\right\}^{4/3} \text{cm}^4 = 31.69 \text{cm}^4$$

The window configuration is also considered to be extremely important. The window should be as wide as possible to maximize winding breadth and minimize the number of layers. This results in minimized leakage inductance. The U and I core shape is chosen for the high frequency transformer. They have large window area in relation to core size, and the window has the desirable wide configuration. For the U 126/91/20 core, the area product can be obtained from the manufactures data sheet. For the of U shape core the following core parameters are obtained.

Effective volume= 268.8 cm^3; Effective length= 48cm; Effective window area of the core, A_w= 5.6 cm^2; Effective core magnetic cross-section area, A_e= 5.6 cm^2

The effective product area of the specified core is $A_p=A_wA_e$=31.36 cm^4. It is observed that the product area of the specified U core closely matches with the product area of the core that has been found from the initial estimated values (31.69 cm^4). In U series core this is the nearest possible value to the required A_p. So this core is selected for the design.

The details high frequency transformers are as specified below:

Transformer core:

Core Material: Ferrite; Core type, Family: UI series, two U cores; Core Size: 126/91/20mm for one U core, 126/182/20mm for two U cores. Input voltage: 560V, 4A; Output voltage: 20V across the secondary winding, 10V across the each secondary winding, 100A; Primary windings: Number of turns: 210 turns; SWG 18; Secondary Windings: Centre-tapped diode bridge rectifier, two secondary windings centre tapped, four turns each winding, Wire strip: Width=20mm, thickness = 0.5mm, Area=10mm^2

III. Control Scheme For The Proposed DC-DC Converter For SMPS

To derive the gating signals for the solid-state IGBT switches for the full-bridge dc-dc converter the reference supply currents along with sensed supply currents are used in the current controllers, which directly generate switching signals.

A. Current- Mode PWM Controller

Fig. 4 shows the control strategy for the full-bridge dc-dc converter based current controlled technique for input current shaping and power factor correction. The voltage error control signal V_{error} is generated by summing the reference dc voltage V_{set} and the sensed dc output voltage V_{dc} is processed by a voltage proportional and integral (PI) controller as shown in Fig. 4.

This is multiplied with the reference dc voltage V_d sampled from the output voltage of the diode-bridge rectifier so that the current reference signal I_{ref} is produced which contains shape information of the voltage, and the output dc magnitude information from the current based PI controller. The feed-forward constant voltage K_v and current sensing K_i are given as,

$$K_v=(1/V_{dmax}) \text{ and } K_i=(1/I_{dmax}) \qquad (32)$$

The sampled dc link current I_d is then compared with the reference current signal and the net error signal between the two is amplified to generate the control signal V_c and it is then compared with a high frequency triangular wave to generate PWM signal.

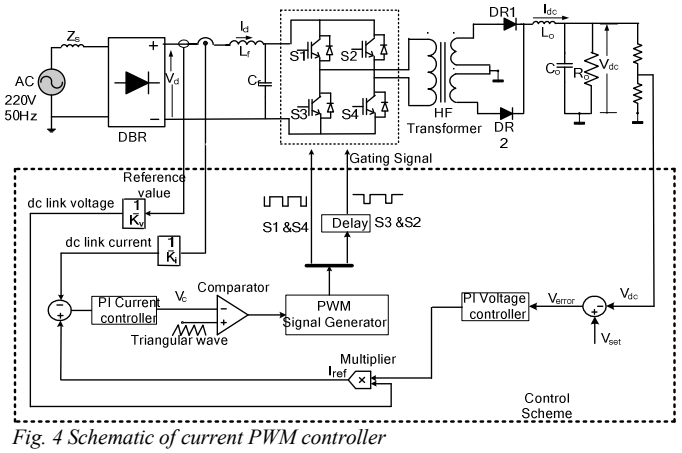

Fig. 4 Schematic of current PWM controller

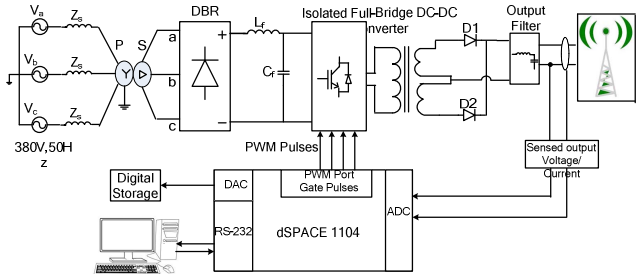

Fig. 5 Schematic diagram of hardware implementation

B. Hardware Implementation of DSP Controller for SMPS

The real time implementation of digital control for a three-phase switched mode power supply is carried out using a fast digital processor (dSPACE DS1104). It mainly consists of a MPC8240 processor with PPC603e core and on-chip peripherals. This is a 64-bit floating point processor with 250MHz central processor unit (CPU) clock frequency.

It also consists of a slave DSP TMS320F240 of Texas Instruments. Fig. 5 shows the schematic diagram of hardware implementation. A DSP controller (DS1104 dSPACE) consists of dSPACE as a master processor and TMS320F240 as slave processor. The following peripherals of the processor are used for the implementation.

1) 4-channel, 12-bit analog to digital converter (ADC) is used to input the sensed output voltage.

2) 8-channel, 16-bit digital to analog converter (DAC) is used to take out the signals from the dSPACE. The DAC channels are used for taking out the PWM pulses being given to the drivers of the IGBT's of the full-bridge converter.

C. Real Time Modeling Using DSPACE

The PWM gating signal for the full-bridge dc-dc converter is built-up with the help of MATLAB Simulink and DSP-dSPACE. The Real Time Interface (RTI) model is built in real-time to generate gating signal for full-bridge dc-dc converter and also to regulate the output dc voltage of the SMPS. The PWM signal generated from dSPACE are fed to the IGBT switches through an isolation and amplifier circuit. Fig. 6 shows the RTI model developed in DSP-dSPACE for PWM generation and PI voltage control. The duty ratio is provided as the input to the main block DS1104SL_DSP_PWM. The PWM duty cycle signals are generated by comparing a level control signal (V_c) with a constant peak repetitive triangle signal (V_{tri}). The frequency of the repetitive triangle signal establishes the switching frequency. The slave DS1104SL_DSP_PWM generates frequency 1.67Hz to 5MHz.

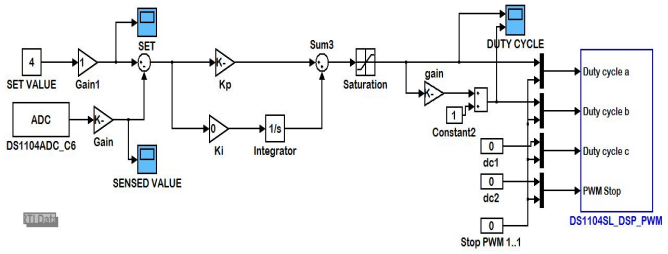

Fig. 6 RTI model of PWM signal generation for full-bridge dc-dc converter

The full-bridge dc-dc converter is operated at a switching frequency of 35 kHz which is internally generated by DS1104SL_DSP_PWM block. The output voltage is sensed by ADC channel 6 of DSP-dSPACE and it is given as the sensed voltage signal to the PI controller as shown in Fig. 6.

IV. PERFOMANCE OF THE PROPOSED DC-DC CONVERTER

In this section, simulation and experimental results of the proposed dc-dc converter are presented. The dynamic performance of the dc-dc converter has been simulated by switching the load suddenly from the steady state condition.

Fig. 7 also shows the dynamic performance of the proposed dc-dc converter under step load conditions from 100% to 20% load and vice versa. It can be observed from Table I that the proposed high frequency converter results in nearly unity power factor in the wide operating range of the load and the input ac mains current THD is between 3.6% and 5.2% under this varying load condition. Moreover, the input voltage THD of the converter is also between 2.4% and 1.2% which is within the standard limits.

To study the performance of the dc-dc converter for SMPS, a single module isolated full-bridge dc-dc converter is developed in the laboratory with the designed components as specified in the previous section. The closed loop voltage control of full-bridge dc-dc converter is implemented using DSP-dSPACE.

TABLE I. POWER QUALITY INDICES FOR THE PROPOSED AC-DC CONVERTER FED SMPS UNDER VARYING LOAD CONDITIONS

Load (%)	v_{THD} (%)	i_{THD} (%)	DPF	DF	PF
20	1.2	5.2	0.9867	0.9981	0.9849
40	1.5	4.9	0.9883	0.9984	0.9868
60	1.8	4.5	0.9897	0.9987	0.9884
80	2.1	4.1	0.9919	0.9991	0.9913
100	2.4	3.6	0.9949	0.9989	0.9938

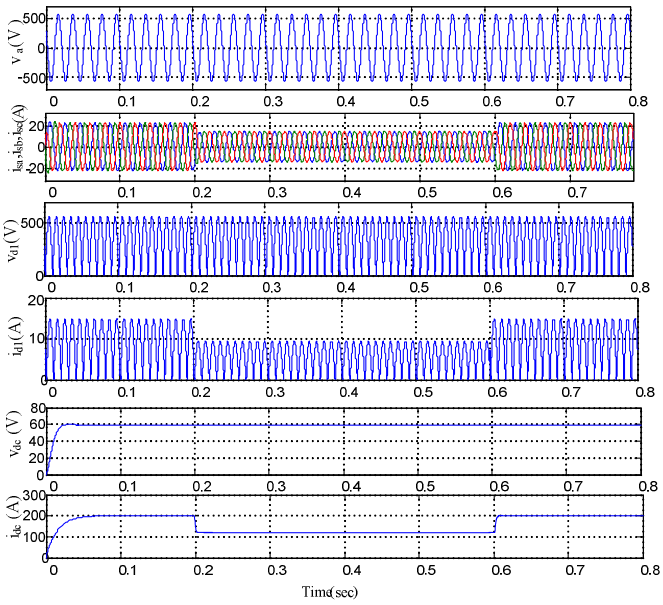

Fig. 7 Simulated results of the proposed high frequency dc-dc converter input currents, dc-link voltage, dc-link current, output current and output voltage waveforms.

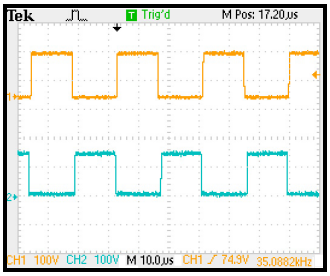

Fig. 8a

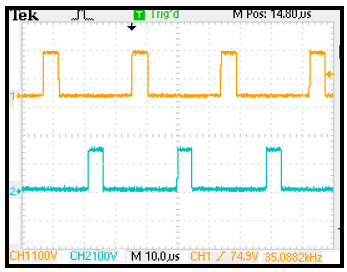

Fig. 8b

Fig. 8 Waveforms of PWM gating signals for full-bridge dc-dc converter

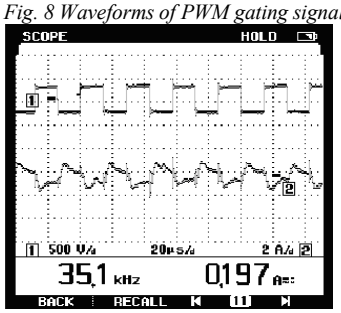

Fig. 9a

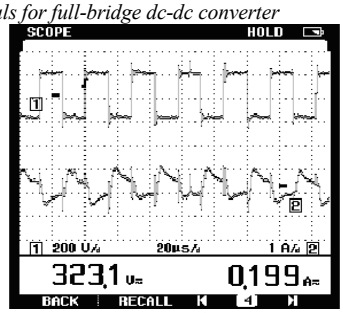

Fig. 9b

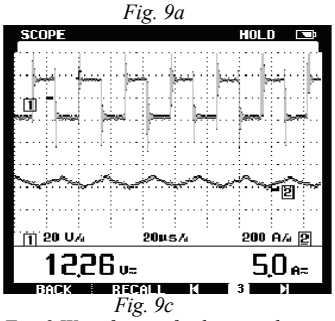

Fig. 9c

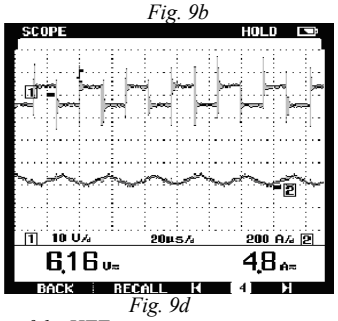

Fig. 9d

Fig. 9 Waveforms of voltage and current of the HFT

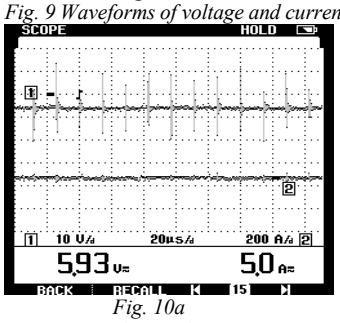

Fig. 10a

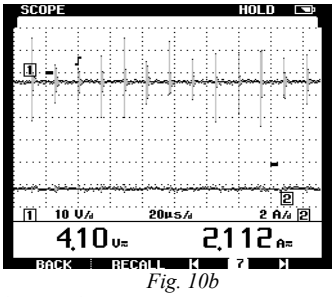

Fig. 10b

Fig. 10 Waveforms of output dc load voltage and current

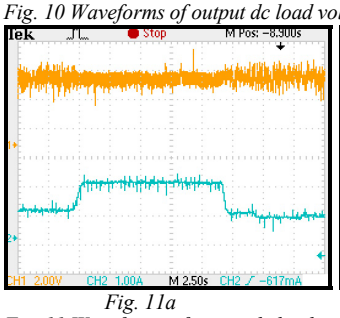

Fig. 11a

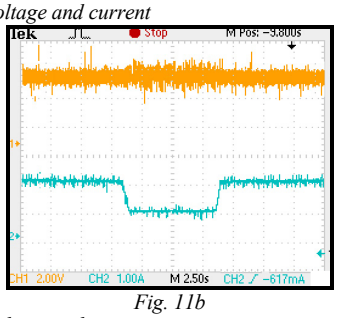

Fig. 11b

Fig. 11 Waveforms of output dc load voltage and current

The laboratory model developed SMPS is tested for 35kHz switching frequency. The PWM switching signal generated by DSP-dSPACE is given to the full-bridge dc-dc converter using isolation optocoupler circuit 6N137. Figs. 8a and b show PWM switching signal for the full-bridge dc-dc converter for two different duty cycles of 0.5 and 0.2 at 35 kHz respectively.

Fig. 9a shows the high frequency transformer parameter switching frequency of 35kHz. Fig. 9b shows the input voltage to the high frequency transformer, peak to peak voltage of 323V square wave generated by the full-bridge dc-dc converter though IGBT switching and input capacitor. Figs. 9c and d show the output voltage of the high frequency transformer of 12.26V peak to peak (across the two output secondary winding) and 6.16V peak to peak (across each secondary winding). The turn's ratio of high frequency transformer being tested of 26:1 in the secondary winding and 4 turns for each secondary winding. Fig. 10 shows the output dc voltage and current for different loads under steady state condition. The slider gain blocks in virtual instruments of DSP-dSPACE Control Desk software is used to vary the real-time gain and view the signals. In closed loop voltage control the PI parameters are tuned to obtain the values and to maintain constant dc voltage across the load. The closed loop control is tested for 4V condition. The parameters of the controller are given below,

K_p= 0.90 and K_i= 0.02 for 4V

Fig.11 shows the response of output waveforms due to sudden variations in the load condition of 4V. It can be observed that the voltage is maintained constant even though there is a sudden variation in the load. Thus PI controller implemented using DSP-dSPACE works well for regulating the dc output voltage.

V. CONCLUSION

An isolated high frequency dc-dc converter based SMPS for telecommunication systems has been described and validated by digital implementation. An average current mode control technique has been used to the proposed converter to provide good load regulation. The proposed high frequency converter for switched mode power supplies has been operated at almost unity power factor, with low THD, and high efficiency. In addition, it has regulated output voltage with wide range of the load variations.

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