SHORT COURSE ON
Modeling and Simulation of Nano-Transistors

FEBRUARY 13 - 17, 2017
Organized by Department of Electrical Engineering, IIT Kanpur

Topics:
- VLSI design and Nanoelectronics
- Physics and Operation of MOSFET
- SPICE and Circuit simulation
- TCAD simulation: Theory and demonstration
- Compact Modeling: Theory and demonstration
- Scaling and Moore’s Law
- International Technology Roadmap for Semiconductors
- Nano-Transistors: FinFET, FDSOI, Negative Capacitance FET
- Characterization: Current and capacitance measurement
- RF CMOS and GaN High Electron Mobility Transistors

Also included:
- Laboratory visits and RF transistor measurement
- New research problems in Nanoelectronics
- How to write research project and papers

Target Audience:
Faculty members, practicing engineers & students.

Website
http://www.iitk.ac.in/nanolab/sc2017

Registration Form
http://www.iitk.ac.in/nanolab/sc2017

Registration Fee **
Faculty: Rs. 10,000
Industry/R&D Labs: Rs. 20,000
Students: Rs. 5,000

Coordinators
Dr. Y. S. Chauhan, IIT Kanpur
Dr. A. Agarwal, IIT Kanpur

Contact
nanolab.iitk@gmail.com

SPEAKERS
A. Dutta
Dept. of EE
IIT Kanpur
Y. S. Chauhan
Dept. of EE
IIT Kanpur
B. Mazhari
Dept. of EE
IIT Kanpur
A. Agarwal
Dept. of Physics
IIT Kanpur
K. V. Srivastava
Dept. of EE
IIT Kanpur
S. S. K. Iyer
Dept. of EE
IIT Kanpur

**Registration Fee includes course fee, accommodation, food, printed lecture notes and stationery.