





SCDT – FlexE Centre Webinar Series

The webinars aim to bring together researchers in Flexible Electronics and allied areas from across India (and other countries) on a single platform to promote professional interaction.

Webinar by



Dr. Subramanian S. lyerDepartment of Electrical and Computer
Engineering, University of California, Los
Angeles, USA

on

"Flexible Hybrid Electronics 2.0"

Date: 16th May, 2023 **Time**: 7:30 PM to 8:30 PM

Visit www.iitk.ac.in/scdt/webinars.html
to access the zoom link to join the webinar.

The event will be chaired by **Dr. Jayanta K. Baral** Central University of Jharkand

Abstract of the Webinar

In the last few years, electronics packaging has rightfully emerged from the shadows of CMOS scaling to make a significant impact in high performance and mobile appliance computing. The area of Flexible Hybrid Electronics (FHE) has also developed and is making a significant impact in the area of medical and wellness electronics. The first generation of these devices have, for most part, adapted Printed Circuit Board (PCB) technology by using thinner PCBs and assembling either thinned or thin packaged "older" generation of chips on to these platforms, typically with coarse printed wiring to connect a small number of such chips. This approach, while immensely useful to get the field going, needs to adapt and borrow from the both silicon and advanced packaging technology trends, so that we can advance this trend to the next level. The key paradigm challenges ahead are: scaling FHE in general - this includes the adoption of dielet (chiplet) technology in more advanced CMOS nodes including edge-AI, higher performance interconnects, flexible high-density energy storage, wireless communication and advanced ergonomics and all of these at lower cost and higher reliability. In this talk we will address these challenges and outline a possible technology roadmap to achieve these goals in the next few years.

Information about the speaker

Subramanian S. Iyer (Subu) is a Distinguished Professor and holds the Charles P. Reames Endowed Chair in the Electrical Engineering Department and a joint appointment in the Materials Science and Engineering Department at the University of California at Los Angeles. He is the Director of the Center for Heterogeneous Integration and Performance Scaling (UCLA CHIPS). Prior to that he was an IBM Fellow. His key technical contributions have been the development of the world's first SiGe base HBT, Salicide, electrical fuses, embedded DRAM and 45nm technology node used to make the first generation of truly low power portable devices as well as the first commercial interposer and 3D integrated products. He has been exploring new packaging paradigms and device innovations that may enable wafer-scale architectures, inmemory analog compute and medical engineering applications.