Model predictive control of DSTATCOM employing a single DC source cascaded H-bridge multilevel inverter in a weak distribution system

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Abstract—This paper presents the performance of distribution static compensator (DSTATCOM) for load compensation in a weak distribution system. The DSTATCOM topology is realized using a single DC source based cascaded H-bridge multilevel inverter (SDCHBMLI). In SDCHBMLI, the multilevel waveform is generated by cascading the output of the transformers connected to individual full-bridge cells. The use of single DC source eliminates the requirement for capacitor voltage balancing, which is one of the limitations of diode-clamped and flying-capacitor based multilevel inverters. Also, the transformers in SDCHBMLI provide inbuilt isolation between the DSTATCOM and the distribution system. In a weak distribution system, feeder impedances make the voltages at point of common coupling (PCC) susceptible to distortions. To improve the PCC voltage waveform, shunt filter capacitors are incorporated in each phase, which make the system more complex to control. In this paper, the DSTATCOM is controlled using Finite Control Set Model Predictive Control (FCS-MPC) technique, which can independently ensure desired compensator current tracking and PCC voltage improvement simultaneously. The operation of proposed DSTATCOM has been verified using PSCAD/EMTDC. The system behavior is simulated for load step changes and voltage sag condition. The robustness of the control algorithm is also validated with variations in model parameters.

Index Terms—DSTATCOM, FCS-MPC, Single DC source based CHBMLI, weak distribution system.

I. INTRODUCTION

With increase in complexity of loads, the problem of maintaining power quality in distribution system is garnering widespread attention. Poor power quality adversely impacts customers and network suppliers by increasing losses and deteriorating the health of connected equipments. Any power quality issues in voltage or current profile translate to a direct financial loss for the consumer [1]. Power Quality issues can be addressed by employing custom power devices in the distribution system. DSTATCOM is a shunt compensating type custom power device. It is used to mitigate power quality problems such as harmonic distortions in the source current, poor power factor and unbalances [2].

The main component of DSTATCOM is a voltage source inverter (VSI) operated in current controlled mode. The VSI can either be a two-level or a multilevel inverter. As compared to two-level inverters, multilevel inverters are gaining popularity because of their numerous advantages. The output waveform of a multilevel inverter is an accumulation of a number of smaller voltage steps. This results in decrease of harmonic content in the output waveform of the inverter, lesser \( \frac{dv}{dt} \), reduction in common mode voltages, smaller filter sizes and operation with a lower switching frequency [3]. A number of multilevel topologies, and their applications are reported in literature [3]-[10].

The most widely used multilevel inverter (MLI) topologies for DSTATCOM applications are diode-clamped (DCMLI) [4], [5]; flying-capacitor (FCMLI) [6], [7] and cascaded H-bridge (CHBMLI) multilevel inverters [8]-[10]. The high requirement of diodes and capacitors increase the design complexities in DCMLI and FCMLI. In both DCMLI and FCMLI, increase in number of levels in the output waveform also increase the number of DC link capacitors. In FCMLI, redundant switching combinations are available which can be utilized for capacitor voltage balancing [6]. Also, for satisfactory operation of the inverters as DSTATCOM, it is important to regulate the voltage of DC link capacitors at desired value. In both cases, higher number of DC capacitors lead to complex voltage balancing methods, either by increasing auxiliary circuits or adding to control constraints. Larger component count increase the converter size and cost. Moreover, the capacitors used in FCMLI need to be pre-charged to the desired voltages before switching [11]. As compared to FCMLI and DCMLI, CHBMLI appears as a convenient choice since it does not require any clamping diodes or capacitors. CHBMLI has a modular structure and the control procedure is easier [8]. One drawback of this topology is the requirement of individual capacitors for each of the full-bridge cells [11]. Usage of individual capacitors require balancing their voltages for a symmetrical multilevel output waveform. Additional controls or circuits have to be designed to balance and equalize the capacitor voltages.

This drawback can be overcome by connecting the individual cells in parallel to the same DC capacitor [12]. In this configuration, the multilevel output waveform of the inverter module is obtained by cascading the output voltages at the secondaries of the transformers connected to each full-bridge cell. This topology is referred to as SDCHBMLI in this paper. SDCHBMLI eliminates the requirement of balancing the capacitor voltages, without compromising the simplicity.
and modularity of the inverter.

For load compensation using DSTATCOM, the switching signals of the VSI are obtained using a closed-loop current control technique. For multilevel inverter based DSTATCOM, various current control techniques like deadbeat control [13], hysteresis control [5]-[9], [14], sliding mode control [10] are used. Deadbeat control is sensitive to variability of parameters in current control loop. Hysteresis control presents some advantages over deadbeat and other control techniques, like simple implementation and faster dynamic response, but it cannot be used in higher order systems [2]. Application of hysteresis controllers for load compensation in systems with feeder impedance is possible by excluding the shunt capacitors, as demonstrated in [9], but the absence of shunt filter capacitors cause distortions in PCC voltages. In most systems with feeder impedance, hysteresis control can be implemented only in conjunction with some other control techniques [4], [10]. This is a major drawback of hysteresis control.

In this paper, a DSTATCOM connected to a weak distribution system is realized using an SDCHBMLI. The control signals for the SDCHBMLI are generated using finite control set-model predictive control (FCS-MPC). Shunt filter capacitors are added at PCC to improve the quality of PCC voltage waveform. Despite the presence of shunt filter capacitors, FCS-MPC can be used independently without the requirement of any other supplementing control methods. Also, the application of FCS-MPC to SDCHBMLI is easier as compared to other control techniques available for MLIs.

The paper is organized into four sections. Section II presents DSTATCOM using SDCHBMLI topology, the DC-link parameter selection, reference current generation and DC-bus voltage control. Current control of the DSTATCOM by FCS-MPC is described in section III. Section IV presents the results and Section V gives the conclusions.

II. DSTATCOM USING SDCHBMLI

A. The SDCHBMLI topology

A distribution system supplying unbalanced loads through feeder impedances is shown in Fig. 1(a). The DSTATCOM is realized using a 7-level SDCHBMLI. It is connected to the PCC through a filter inductor \( L_f \) and a capacitor \( C_f \). The SDCHBMLI consists of three single-phase inverter modules supplied from a common DC-link capacitor \( C_{dc} \). Each single phase module consists of three full-bridge cells, as shown in Fig. 1(b). The output from each cell is connected to the primary of a transformer. The output waveform of each inverter module is a series combination of the transformer secondary voltages, given by,

\[
v_{ox} = v_{x1} + v_{x2} + v_{x3}, \quad x \in (a, b, c) \tag{1}
\]

The switching logic combinations for a single cell is shown in Table I, where \( k \in (1, 2, 3) \). The output voltages of an individual inverter module are shown in Table II, where \( S_x \) indicate the level of the inverter operation.

B. DC link parameter design

The compensation capability of DSTATCOM is dependent on the average DC-link voltage, \( V_{dc} \), which can be selected to be higher than two times the peak phase voltage [18]. Thus, for a two-level inverter,

\[
V_{dc} = \frac{2 \sqrt{2} V_{LL}}{\sqrt{3}} \tag{2}
\]

As the output voltage of SDCHBMLI is in integral steps of the DC-link voltage, for an N-level SDCHBMLI,

\[
V_{dc} = \frac{2 \sqrt{2} V_{LL}}{M \sqrt{3}}, \quad M = \frac{(N-1)}{2} \tag{3}
\]
Thus, $V_{dc}$ reduces by ‘M’ in case of a DSTATCOM realized using SDCHBMLI.

Depending upon the kVA rating of the system and DC link voltage, the required capacitance of DC capacitor, $C_{dc}$, can be obtained. If $X$ be the kVA rating of the system, let the compensator be capable of handling a ±50% variation in the system rating for $n$ cycles. In this time, let the DC link voltage be allowed to undergo a ±20% change in its value. With the fundamental cycle of the system being $T$ seconds, $C_{dc}$ is calculated as [14]

$$C_{dc} = \frac{2(X - \frac{X}{2})nT}{(1.2V_{dc})^2 - (0.8V_{dc})^2}$$

(4)

C. Reference Current Generation

The compensator is operated in current controlled mode for distortion reduction, power factor improvement and unbalance elimination. For current controlled operation, the inverter output should track a pre-evaluated set of reference currents. Instantaneous symmetrical components theory is applied to calculate the reference currents. As only the real power demanded by the load should be drawn from the source, the desired reference source currents for a system without feeder impedance are given by [2]

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \frac{1}{\sum_{x=a}^3 v_{x}^2} \begin{bmatrix} 1 & 1 & -1 \\ 1 & 1 & 1 \\ 1 & -1 & 1 \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \left( p_{loss} + p_{avg} \right)$$

(5)

where $p_{avg}$ is the active power consumed by the load and $p_{loss}$ is output from the DC bus voltage controller, discussed in subsection-II-D. In a weak distribution system, due to the presence of feeder impedance, source voltages ($v_{sa}$) and PCC voltages ($v_{tx}$) have different values. Also, unbalance in the loads is reflected at PCC voltages. Hence if $v_{sx}$ is replaced with $v_{tx}$ in (5), the resultant reference source currents will be unbalanced, nullifying the objective of DSTATCOM. Hence, in a weak distribution system, fundamental component of the positive sequence PCC voltages ($v_{tx}^{+}$) are utilized to generate the reference currents,

$$\begin{bmatrix} i_{sa}^+ \\ i_{sb}^+ \\ i_{sc}^+ \end{bmatrix} = \frac{1}{\sum_{x=a}^3 v_{tx}^{+2}} \begin{bmatrix} 1 & 1 & -1 \\ 1 & 1 & 1 \\ 1 & -1 & 1 \end{bmatrix} \begin{bmatrix} v_{ta}^+ \\ v_{tb}^+ \\ v_{tc}^+ \end{bmatrix} \left( p_{loss} + p_{avg} \right)$$

(6)

The unbalanced terminal voltages are converted to its sequence components using symmetrical transformation

$$\begin{bmatrix} v_{0}^- \\ v_{1}^+ \\ v_{2}^- \end{bmatrix} = \frac{1}{\sqrt{3}} A \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} \quad A = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix}$$

(7)

The fundamental of the sequence components are extracted using Fourier transformation [2],

$$v_{11}^+ = \frac{\sqrt{2}}{T} \int v_{i1}^+ e^{-(w_{c} - \frac{\pi}{2})} dt, \quad T = \frac{\omega}{2\pi}$$

(8)

The fundamental component of the symmetrical components are subjected to an inverse transformation to generate the fundamental components of the PCC voltages.

$$\begin{bmatrix} v_{ta1}^+ \\ v_{tb1}^+ \\ v_{tc1}^+ \end{bmatrix} = A^{-1} \begin{bmatrix} v_{0}^+ \\ v_{1}^+ \\ v_{2}^- \end{bmatrix}$$

(9)

At PCC, reference compensator currents, $i_{f,cx}^+$, are given by

$$i_{f,cx}^+ = i_{ct} - i_{cx}^*$$

(10)

From Fig. 1(a), the reference current for the DSTATCOM, $i_{f,cx}^*$, is

$$i_{f,cx}^* = i_{fx}^* + C_f \frac{dv_{tx}}{dt}$$

(11)

The model predictive current control ensures that the voltages at PCC are equal to their fundamental positive sequence components, $v_{tx} = v_{tx}^{+}$.

D. DC bus voltage control

The voltage of the DC-link capacitor should be maintained at the desired value under disturbances. To control the aforementioned voltage at the required value calculated in (3), a PI controller is commonly used. The error between the reference DC-link voltage, $V_{dcref}$ and the averaged capacitor voltage, $V_{dc}$, is fed into a proportional-integral controller as depicted in Fig. 2 [17]. The output from the control loop is $p_{loss}$ which is the real power drawn by the compensator from the source to sustain the DC-link capacitor voltage at the desired value. This term is used in (6) for reference current generation.
III. PREDICTIVE CURRENT CONTROL

The predictive control methods utilize the explicit mathematical model to predict subsequent responses of system. The cost function, which gives a measurement of error between the reference value and predicted value of the desired output variable, is minimized to generate the control signals [15]. The advantages of MPC method are fast response in transient states, possibility of multi-objective cost function, and easier inclusion of non-linearities [16]. The particular benefit of implementing predictive control for load compensation in systems with feeder impedance is that it overcomes the problems posed by hysteresis control. Hysteresis control alone cannot ensure stability in distribution networks that includes shunt capacitor filters and generally requires inclusion of another control technique [2], [4]. Predictive control can be independently implemented in a weak distribution system with shunt capacitors. A deterrent against predictive controls is the large computational demand due to requirement of optimizing the cost function. To circumvent this problem, FCS-MPC is used. In this method, the finite combinations of switching states that are possible in a converter are exploited to reduce the computation load.

In the application investigated in this paper, the 7-level SDCHBMLI has to be operated so that the actual output current from the inverter, \( i_{f cx} \), tracks reference current \( i^*_{f cx} \) as determined in (11). The schematic for the proposed FCS-MPC method is outlined in Fig. 3. The mathematical model for predicting the values of DSTATCOM currents at next sampling instants is obtained by applying KVL in Loop 1, as shown in Fig. 4,

\[
-S_x V_{dc}(k) + L_f \frac{d i_{f cx}(k)}{dt} + R_f i_{f cx}(k) + v_{tx}(k) = 0 \tag{12}
\]

If \( T_s \) is the sampling time interval, then in discrete time domain,

\[
\frac{d i_{f cx}(k)}{dt} \approx \frac{i_{f cx}(k) - i_{f cx}(k-1)}{T_s} \tag{13}
\]

Fig. 3. Schematic of Model predictive control of DSTATCOM

Fig. 4. Single-phase equivalent circuit diagram

Fig. 5. Flowchart for determining switching sequences according to FCS-MPC

Thus (12) can be written as

\[
-S_x V_{dc}(k) + L_f \frac{i_{f cx}(k) - i_{f cx}(k-1)}{T_s} + R_f i_{f cx}(k) + v_{tx}(k) = 0 \tag{14}
\]

The value of \( i_{f cx} \) at \( k^{th} \) sampling instant is obtained from (14)

\[
i_{f cx}(k) = \frac{1}{1 + \frac{T_s}{L_f}} i_{f cx}(k-1) + \frac{1}{R_f + \frac{T_s}{L_f}} \left[ S_k V_{dc}(k) - v_{tx}(k) \right] \tag{15}
\]

Predictive control requires the value of \( i_{f cx} \) at the \((k+1)^{th}\) instant. Thus, advancing (15) by one sampling instant, the predicted value of \( i_{f cx} \) denoted by \( i_{f cx}(k+1) \), is given by

\[
\hat{i}_{f cx}(k+1) = \frac{1}{1 + \frac{T_s}{L_f}} i_{f cx}(k) + \frac{1}{R_f + \frac{T_s}{L_f}} \left[ S_k V_{dc}(k+1) - v_{tx}(k+1) \right] \tag{16}
\]

The switching combination, \( S_{x_{opt}} \), corresponding to the minimum \( g_x \) is applied to the inverter. If \( T_s \) is sufficiently small, then, \( v_{tx}(k+1) \approx v_{tx}(k) \), \( i^*_{f cx}(k+1) \approx i^*_{f cx}(k) \) [19].

IV. RESULTS

The performance of DSTATCOM realized with a 7-level SDCHBMLI is investigated using PSCAD/EMTDC with the simulation parameters given in Table III.
TABLE III
SIMULATION PARAMETERS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source voltage</td>
<td>11 kV, line-to-line RMS</td>
</tr>
<tr>
<td>Feeder impedance</td>
<td>$(1 + j5.14)\Omega$</td>
</tr>
<tr>
<td>Filter parameters</td>
<td>$R_f = 1.01\Omega$, $L_f = 3.5, mH$, $C_f = 10, \mu F$</td>
</tr>
<tr>
<td>Transformer parameters</td>
<td>1 : 1, 2.5 MVA</td>
</tr>
<tr>
<td>DC link voltage</td>
<td>6500 V</td>
</tr>
<tr>
<td>DC link capacitance</td>
<td>$4400, \mu F$</td>
</tr>
<tr>
<td>Sampling time, $T_s$</td>
<td>$10, \mu S$</td>
</tr>
</tbody>
</table>

The system is supplying a load of $(30 + j94.24)\, \Omega$, $(60 + j62.83)\, \Omega$ and $(70 + j31.46)\, \Omega$ in phases $a$, $b$ and $c$ respectively. A three-phase uncontrolled rectifier with an RC load of $50\, \mu F$ and $500\, \Omega$ is also connected at PCC.

Fig. 6. Optimum switching level $S_{a_{opt}}$ of phase-$a$

Fig. 7. Output of individual full-bridge cells and phase-$a$ inverter module

Fig. 8. Uncompensated system response: Unbalanced source currents (top), scaled terminal voltage ($v_{ta}/50$) and source current in phase-$a$ (bottom)

The output from the controller, $S_{x_{opt}}$ is plotted in Fig. 6. The voltage levels at which each inverter module should operate is determined by $S_{x_{opt}}$ according to Fig. 3 and Table II. The switching signals are then chosen as per Table I. The output of the individual full-bridge cells and the inverter module for phase-$a$ is shown in Fig. 7. For example, when $S_{a_{opt}}$ is $+1$, $v_{oa}$ is $+v_{dc}$ and when $S_{a_{opt}}$ is $-2$, $v_{oa}$ is $-2v_{dc}$ and so on.

The unbalanced and distorted source currents in the uncompensated system is plotted in Fig. 8. The scaled PCC voltage of phase-$a$ and source current $i_{sa}$ are plotted to exhibit poor power factor of the load. It can also be noted that the effect of feeder impedance is reflected in the distortion creeping into PCC voltages. The compensated system response in which the source currents become balanced and distortion free is shown in Fig. 9(a). It is seen that source current in phase-$a$ is in phase with the PCC voltage. The PCC voltage becomes free from distortions in the compensated system as compared to Fig. 8. A step change is given in the load current in phase-$c$ at 0.35 seconds. The source currents continue to remain balanced and sinusoidal even after change in load. The total harmonic distortion in source currents in each phase of the compensated system reduces to $1\%$. Thus the objective of mitigating unbalance and distortions in source currents while preserving the quality of PCC voltages, taking feeder impedance into consideration, is achieved by the DSTATCOM. Fig. 9(b) gives the performance of FCS-MPC technique. It is observed that the measured source currents and DSTATCOM currents are tracking the reference source and DSTATCOM currents respectively.
optimum switching sequence by exploiting the finite possible switching combinations for reference tracking. The DSTATCOM is successful in eliminating unbalance, harmonics and improving power factor of the load, along with maintaining a clean PCC voltage. The performance is tested with step changes in load and sag in source voltage. The FCS-MPC technique is verified by subjecting it to deviations in the filter parameters.

V. CONCLUSION

A three-phase DSTATCOM is realized with a 7-level SD-CHBMLI. A mathematical model of the system for application of FCS-MPC is derived utilizing the quantities that are available at the PCC. The algorithm is presented for selecting the

REFERENCES