Enhanced Alpha Plane Line Protection

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***Abstract*- The ratio of currents at both ends of the transmission line is utilized in alpha plane differential principle to detect an internal fault. Such a scheme uses either phase current or sequence currents. As the ratio computed using phase current and sequence currents has their own demerits, both are combined to enhance the security and sensitivity of the protection scheme. However, such a scheme which uses both phase and sequence current demands large communication channel requirement and has limited performance during high resistance fault during single pole tripping and Metal oxide Varistor (MOV) operation in series compensated line. In this work, phase current based adaptive alpha plane differential protection scheme is proposed which uses change in current and phase angle between voltage and current at both ends of the line. The proposed method is tested for Western-System-Coordinating-Council 9-bus system and results show it works for all circumstances and it is also valid for series compensated line.**

***Index Terms*— Current transformer; capacitor coupled voltage transformer; Digital Relay; Global positioning system; Series compensation;**

I. Introduction

Differenatial relaying which uses both end data has limited performance for long transmission line due to the latency and charging current. In the advent of microwave and direct fiber-optic communications [1]-[2], data availability from other end is feasible. This has opened new doors of differential protection even for long transmission lines. Such both end data based schemes have inherent immunity to power swing, mutual coupling and series impedance unbalances and improves security of the system [3]. However the performance is compromised during CT saturation and loses its sensitivity to high resistance fault and seeks external supervision using additional features which can prevent such maloperations. This is possible in digital relaying which can adapt the decision in accordance with system condition.

Directional comparison based scheme which requires voltage and current data from both sides of the line is widely adopted in power system [4]. However the performance of such scheme is compromised during voltage signal distortion for close-in faults or blown fuses, ferro-resonance problems in voltage transformers and transients in capacitor coupling voltage transformer (CCVT) [5]. A technique which uses both ends current provides a solution to such issues. Among the current based techniques phase comparison, charge comparison, and current differential schemes are well known [6]. However, such techniques are sensitive to intercircuit, cross country fault and has setting limitations during current transformer saturation. The threshold setting is difficult which varies with system condition [7].

Now-a-days with the help of Global Positioning System current phasors are obtained and applied for differential relay. This provides immunity to channel delays and asymmetry [8]-[10]. Synchronized phasors are also utilized to eliminate the errors caused by charging current for high voltage transmission line [11]. In [12], an adaptive restraining quantity is derived using the synchronized currents to improve the stability and sensitivity. Power from both ends of the line is also applied to detect the internal fault [13]. However such schemes have limited performance when GPS signal is interrupted and this is not under the control of the protection engineer.

In [14]-[15], alpha plane, a geometric representation in the complex plane is proposed which computes the ratio of the phase or sequence currents at both ends of transmission line to detect internal fault. It has important advantages such as: significant tolerance to CT saturation and synchronization errors. Phase current based Alpha plane scheme maloperates during high resistance fault and weak source condition. The sequence current based schemes are sensitive to high resistance faults but they are limited to single pole operations and line impedance dissimilarity during the MOV operation in series compensated lined. In [16], negative, zero and phase currents are applied to improve the sensitivity and stability of alpha plane relaying. A modified alpha plane characteristic is proposed to improve the sensitivity [17]. During single pole tripping new sequence element logic is adopted to improve the sensitivity of the relay in alpha plane [18].

In this work, phase current based technique is developed which has improved performance for high resistance fault and series impedance unbalances. In the proposed method, the phase angle between the voltage and current and magnitude of change in current from both the ends are utilized to compute modified current ratio which has better performance for high resistance fault, current transformer saturation, single pole tripping. The proposed method is tested for WSCC 9-bus

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system with and without series compensated line. Simulation results show the accuracy of the proposed method.

II. Alpha Plane Characteristic For Line Protection

The two bus system as in Fig 1 is considered to describe the current differential scheme. For any operating condition both end current phasors are taken and ratio is computed as,

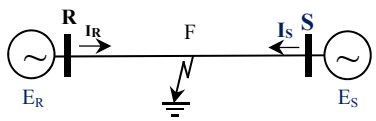

Fig. 1. Two source equivalent system.

$$\frac{\dot{I}_S}{\dot{I}_R} = ke^{j\alpha} \tag{1}$$

where k is the magnitude and α is the phase angle difference between currents at R and S sides as in Fig. 1. The alpha plane characteristic is provided in Fig. 2.

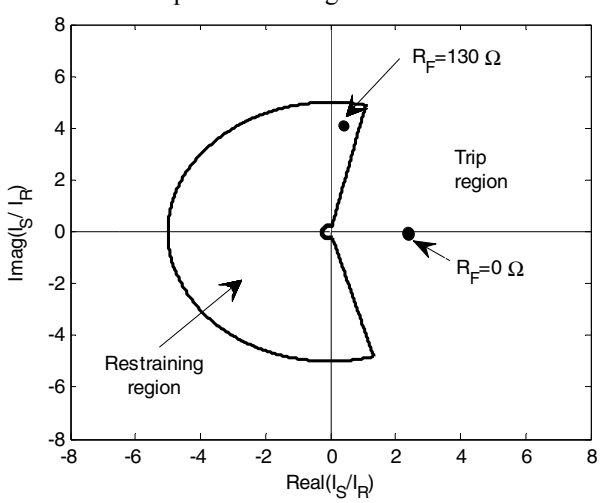

Fig. 2. Differential characteristic in current ratio plane.

During normal operating condition the locus of current ratio remains within the boundary which is the restraining region as in Fig. 2. During any disturbance the locus moves out of the restraining region the scheme declares it as an internal fault. The characteristic is set considering two parameters: the radius R of the greater arc (5<R<10) and the angle alpha(α) (160° < α <210°)[15]. In this case to incorporate the communication delay and errors due to CT saturation alpha is selected as 210° and the radius of greater arc is selected as 5.

The phase based differential relay has limited performance during high resistance fault and sometimes the locus for high resistance fault during heavy loading condition enters into the restraining region. To test such an event a 250 km line between R and S with a load angle of 35˚ is considered. With a fault resistance R_f=0Ω when a line-to-ground fault is simulated in EMTDC/PSCAD at 50 km from S bus and the current ratio is plotted in Fig.2, the locus remains in operating region. As the fault resistance is increased gradually the locus of current ratio moves towards the restraining region. It is observed that with R_f=130Ω the locus have completely entered into the restraining region. Even though it is a fault, the conventional scheme interprets it as a healthy condition and this is a maloperation. Additional features are required to prevent maloperation of alpha plane characteristic. As resistive part increases for high resistance fault in the fault loop the angle between voltage and current varies with fault resistance. This indicates power factor angle is a good indicator of high resistance fault and this is utilized in the proposed method to prevent maloperation during such type of fault.

III. Proposed Method

Phase current based alpha plane differential relay has numerous advantages like immunity to CT saturation and channel asymmetry. The main challenge is prevent the maloperation of the scheme during high resistance fault. During higher loading condition when high resistance fault occurs the phase angle between voltage and line current is modulated and it is different from the line impedance angle. The deviation in phase angle from impedance angle indicates fault resistance is high and this is utilized to modify the computation in (1) during such events.

$$f(\alpha) = \frac{\dot{I}_S}{\dot{I}_R}\, e^{(-jK_1(\emptyset_1+\emptyset_2)} \tag{2}$$

Where $\emptyset_1$ and $\emptyset_2$ are the phase angle deviation from transmission line impedance angle at both ends of the transmission line. This can be computed with known values X and R for transmission line and phase angle between the voltage and current at S and R buses. K_1 will be set as 1 or 0 depending on the rule given below.

$$K_1 = \begin{cases} 0 & if\ \emptyset_{min} < \emptyset_{th} \text{ or } (\Delta I) < \in \\ 1 & if\ \emptyset_{min} > \emptyset_{th} \text{and } (\Delta I) > \in \end{cases} \tag{3}$$

$\emptyset_{min}$ and ΔI are the two criteria chosen to discriminate external, internal high resistance fault and normal operating condition. $\emptyset_{th}$ and $\in$ are the thresholds selected for $\emptyset_{min}$ and ΔI respectively.

The change in phase angle $\emptyset_1$ and $\emptyset_2$ at both ends of the line is considered to discriminate high resistance fault condition to normal operating condition. As the change in phase angle for both internal and external high resistance fault is similar, the deviation of voltage and current phase angle from line impedance dose not conclude internal and external high resistance fault. For any external fault or load increment, the magnitude of change in current at both ends of the line is equal. To differentiate the internal and external high resistance fault another criteria difference in magnitude of change in current at both ends of the line is selected. The difference in magnitude of change in current at both ends is expressed as,

$$\Delta I = abs(\Delta I_S) - abs(\Delta I_R) \tag{4}$$

However during CT saturation, the current difference will be high but the phase angle change $\emptyset_1$ and $\emptyset_2$ may not be

significant at both ends. For this reason minimum of both ends phase angle deviation is considered to discriminate high resistance fault from CT saturation and $\emptyset_{\min}$ is expressed as,

$$\emptyset_{\min} = \min(\emptyset_1, \emptyset_2) \tag{5}$$

Similarly during external high resistance fault change in phase angle are significant but ΔI is negligible. Both the features are combined to detect the internal high resistance fault and relation (1) is modified whenever it is required. The

Next section describes the threshold selection criteria for the features.

A. *Threshold selection criteria for* ΔI.

Phase angle deviation indicates a high resistance fault but it cannot confirm internal or external fault. During normal operating condition and external fault current entering to the line is equal to leaving current. Current magnitude can be selected as parameter which can external or internal fault. Shunt capacitance may cause in variation in current magnitude at both the ends. For this reason magnitude of change in current is considered, where effect of shunt capacitance is nullified. There may be difference in current ΔI during normal loading condition due to CT error. This is considered in threshold setting to discriminate high resistance internal fault to load change condition. Considering the 2 % error for C class CT at both the ends [19] and to provide a secured operation a threshold ε is selected as 0.08 pu.

B. *Threshold selection criteria* $\emptyset_{th}$

External and internal high resistance faults can be distinguished by using ΔI . During CT saturation the change current at both ends are same and ΔI will be of significant. Further CT saturation occurs in case of low resistance fault and change in phase angle at the remote end is less compared to relay end. At remote end the deviation in phase angle between voltage and current from the transmission line impedance angle depends only on shunt capacitance. Knowing the line length a threshold for $\emptyset_1$ and $\emptyset_2$ can be set which can indicate high value of ΔI is caused due to CT saturation. For proper operation of the scheme it is required to use both phase angle change and ΔI.

Considering an external line-to-ground fault beyond S bus two source equivalent system as in Fig. 1, the phase angle deviation is observed and from which the threshold for $\emptyset_{th}$ is selected. The source voltages at bus R and S at any operating condition can be expressed as,

$$\frac{\dot{E}_{\mathrm{R}}}{\dot{E}_{\mathrm{S}}} = he^{-j\delta} \tag{6}$$

where h magnitude ratio and δ is the angle difference. Using h and δ fault current for line-to-ground fault with R_F= 0 Ω beyond S bus in Fig. 1 can be computed and the fault current at bus R can be expressed as,

$$I_{\mathrm{aR}} = I_{\mathrm{pre}} + I_{1\mathrm{L}} + I_{2\mathrm{L}} + I_{0\mathrm{L}} \tag{7}$$

Similarly, the voltage at the bus relay can be computed as,

$$V_{\mathrm{aR}} = 3R_{\mathrm{F}}I_{\mathrm{F}} + \left(2I_{1\mathrm{L}} + \mathrm{I}_{\mathrm{pre}}\right)(\mathrm{Z}_{1\mathrm{L}}) + I_{0\mathrm{L}}(Z_{0\mathrm{L}}) \tag{8}$$

The phase angle between V_{aR} and I_{aR} can be computed for different operating conditions. The source impedances are varied and the impact on phase angle is observed. The variations in voltage and current angle depend on line length and line parameters.

The variation in phase angle depends on prefault loading condition and both end source impedance. To observe the effect of source impedance variation on phase angle between voltage and current, the source impedance at one end is varied from 0.2 pu. to 2 pu[21].. The variation of $\emptyset_1$ is observed and the maximum value is found as 0.362 radian.

Similarly the maximum deviation of phase angle is observed for h and δ. Magnitude ratio is varied from 0.9-1.1 pu. and δ is varied form 0- 35˚. The maximum deviation of phase angle at R bus for h and δ variations is observed as 0.362 and 0.4178 radian respectively. From all these observations the threshold $\emptyset_{\mathrm{th}}$ is selected as 0.436 radian.

C. *Flow diagram of the Proposed Method*

The flow diagram of the proposed method is shown is Fig 4. The input to the scheme is voltage and current phasor data from both ends of the line. In first step both ends current ratio is calculated using (1). Whenever locus is inside the restraining area the scheme computes the change in current ΔI . When the change in current is more than the predefined threshold ε, the minimum of Φ_1 and Φ_2 is calculated. The minimum value is compared with Φ_{th} and if it is more than the threshold, K_1 is set as 1 and current ratio is calculated using (2). During fault even though phasor computation is affected by decaying DC, it does not affect the decision process as the difference in line impedance angle and angle between voltage and current is more. The scheme performs well during power swing as ΔI is low during these conditions.

IV. Simulation Results

The 230 kV, 60 Hz WSCC 9-bus system as shown in Fig.5 [20] systems are used to test the effectiveness of the proposed method. The line connected between 4 and 5 busses are selected The system is simulated in EMTDC/PSCAD for various system conditions such as internal and external high resistance line-to-ground and double-line-ground fault, CT saturation, load increment and among them few cases are provided in this section. The method is also tested for series compensated lien. Current phasors are obtained by using one cycle Discrete Fourier Transform (DFT). Data sampling rate is maintained at 1.2 kHz.

A. *Case-1: Test for Internal High Resistance fault*

The prefault power is flowing from bus 7 to 8. To test the proposed method a line-to-ground fault with R_F =200Ω is simulated at 5 km from the bus 7 on the line connecting

between the buses 7 and 8. The voltage and current phasors are obtained and ΔI is calculated and plotted in Fig. 6 (a). The increased value of ΔI form the preset threshold triggers the proposed scheme and phase deviations are calculated and minimum of both the phase angle are plotted in the Fig. 6 (c). As the Φ_{min} is more than the Φ_{th} K_1 is set as 1 and the current ratio is calculated using (2). Current ratio calculated by both the conventional and proposed method is plotted in Fig. 7. From the figure it is observed that the conventional current ratio remains inside the restraining region and at the same time the current ratio using the proposed method shift to operating region. This reveals correct operation of alpha plane characteristic using the current equation by proposed method.

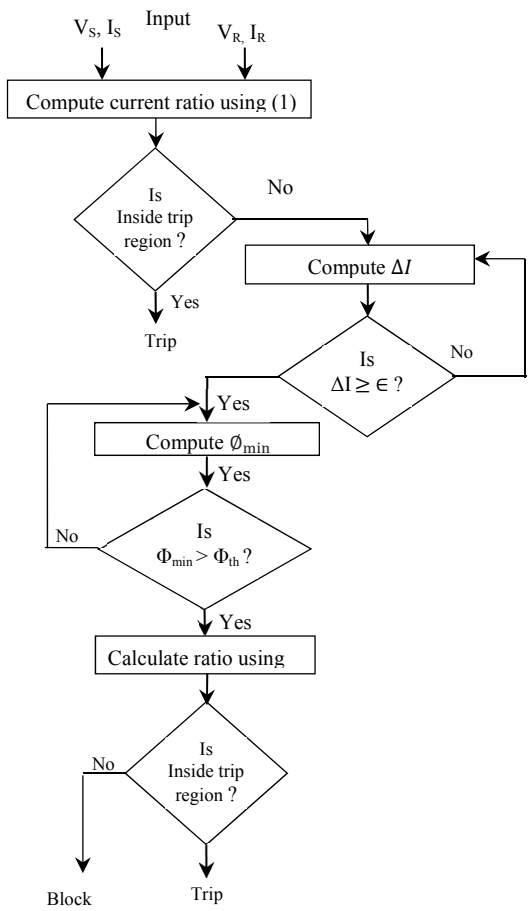

Fig. 4. Flow diagram for proposed algorithm.

B. Case II. Test for External High Resistance Fault

The proposed method is tested for external line-to-ground fault with R_F =200Ω is simulated at 5 km from the bus 8 on the line connecting between the buses 8 and 9. The voltage and current phasors are obtained and ΔI is calculated and plotted in Fig. 8 (a). The increased value of ΔI from the preset threshold triggers the proposed scheme and phase deviations are calculated and minimum of both the phase angle are plotted in the Fig. 6 (b). As the Φ_{min} is more than the Φ_{th} K_1 is set as 0 and the current ratio is calculated using (1). Current ratio calculated by both the conventional and proposed method is plotted in Fig. 9 which reveals both methods provide correct result.

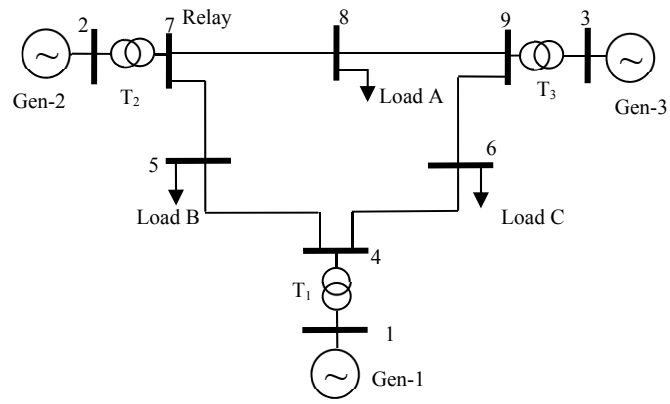

Fig. 5. WSCC 9-bus system for testing α-plane relay at bus 7 for line 7-8.

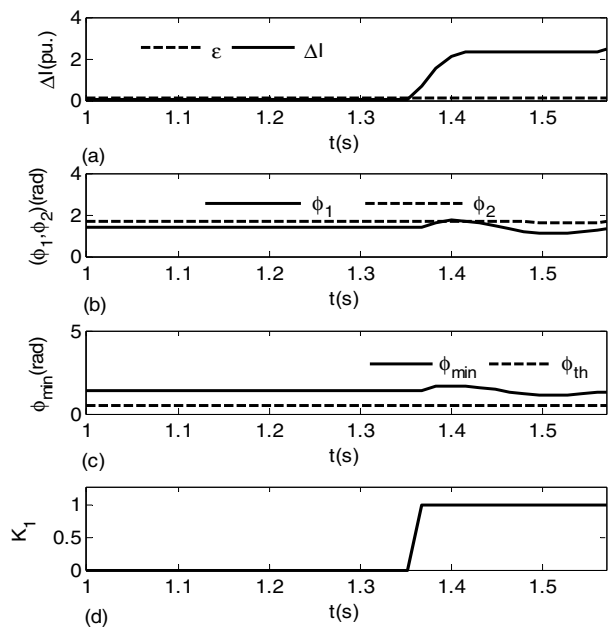

Fig. 6. Indices for internal line-to- ground fault with R_F = 200 Ω. (a) ΔI increment (pu.). (b) Φmin (rad).(d) Index K_1.

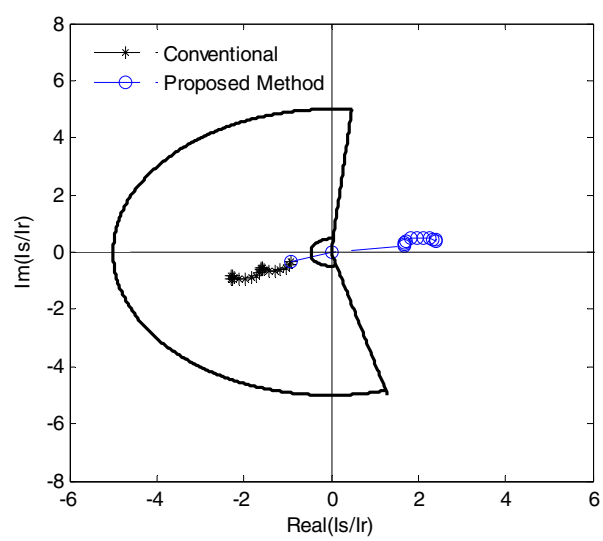

Fig. 7. Alpha plane characteristic for internal line-to-ground fault with R_F = 200Ω.

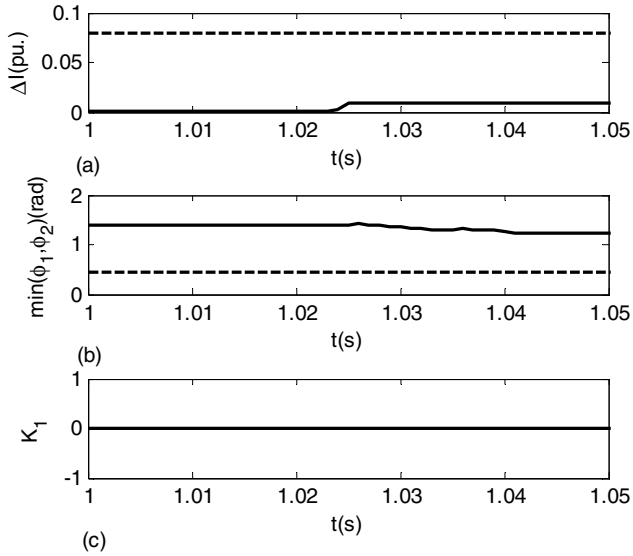

Fig. 8 Indices for external line-to- ground fault with R_F = 200 Ω. (a) ΔI increment (pu.). (b) Φmin (rad).(c) Index K_1.

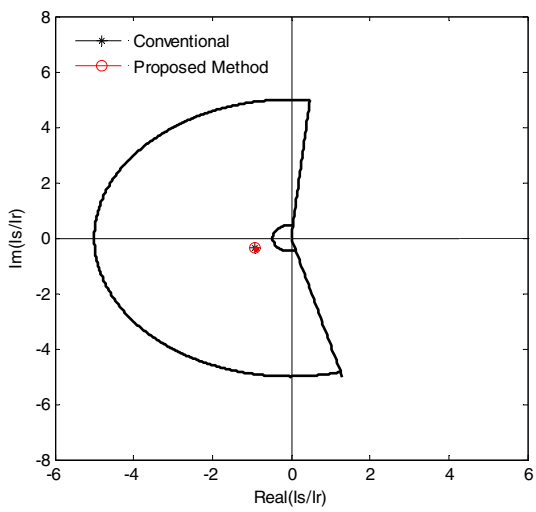

Fig. 9. Alpha plane characteristic for external line-to- ground fault with R_F = 200 Ω.

C. *Test for Load change*

As change in current at both ends of the line is considered as input to the proposed scheme, the accuracy of the method is tested for load change. The load connected to bus-8 is increased by 50 MW at 2.4 s. The current ratio computed using (1) is plotted in Fig. 11 and it settles inside the restraining region. During this period ΔI for the line 7-8 is plotted in Fig. 10. It is observed $\Delta I < \varepsilon$ which computation of Φ_{min} is not required. This implies as per (3) K_1=0. The current ratio computed using (2) is also plotted in Fig. 11 and both ration computed by conventional and proposed scheme remains in the restraining region. Thus, the method works accurately for load change also. During unbalance loading also the method performs correctly as the phase currents are taken as inputs. Negative and zero sequence component based method has limitations for unbalance loading condition.

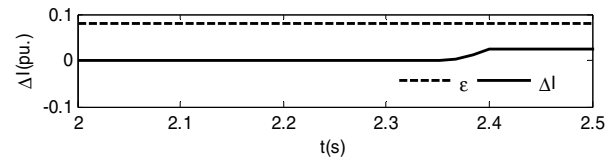

Fig. 10. Result for load change case ΔI (pu.).

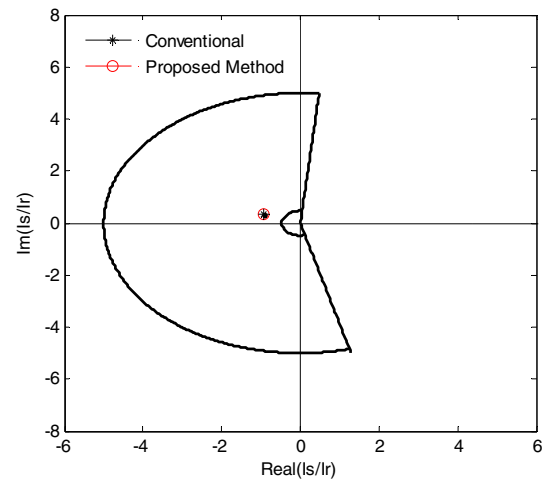

Fig. 11. Alpha plane characteristic for load increment.

D. *Test for Series compensated line*

MOV protected series compensated line introduces challenges to existing protection schemes. The MOV operation depends on fault resistance, type of fault, prefault current and distance up to the fault point. Operation of MOV introduces asymmetry in the phase impedances [18] and computation of the sequence components becomes erroneous. This makes proposed phase based approach advantageous than the conventional method.

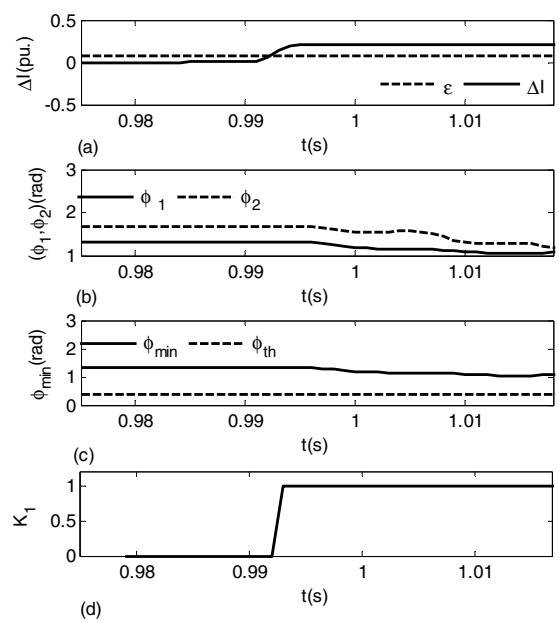

Fig. 12. Result for high resistance fault in series compensated line (a) ΔI (b) Phase angle deviation at both ends. (c) Φmin (d) Index K_1.

The accuracy of the proposed method is tested with different compensation level and location of the line. Among them one case is presented with a 40% series compensation

is considered in line 7-8, at bus 7 of Fig. 4. The rating of MOV is selected as in [12]. A line-to-ground fault with R_F =200 Ω, at 5 km from the bus 8 on the line 7-8 is created at 0.99s. As observed form Fig. 13, the current ratio computed by conventional method remains in restraining region. ΔI is computed with phase angle change at both ends of line . From Fig. 12, the computed index shows K_1=1 during the fault and the current ratio computed using (2) is plotted in the Fig. 13 which settles outside the restraining region. This confirms the proposed scheme identifies it as an internal fault which is correct.

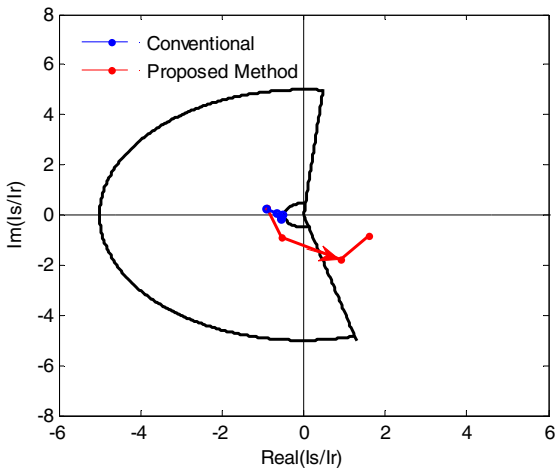

Fig. 13. Alpha plane characteristic for internal high resistance fault in series compensated line.

V. Conclusions

Phase current based alpha plane relay has limited performance during high resistance fault. In this work computed ratio is modified using change in current and the phase angle between the voltage and current at both ends of the line. The proposed scheme is tested for numerous cases with and without series compensated line. The results show the sensitivity of the conventional scheme has improved and performs correctly for high resistance fault in a series compensated line. The proposed method tested for 9 bus system results show the methods works accurately.

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