An Improved Power Quality Induction Heater Using Zeta Converter

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***Abstract*—This paper presents an induction heater (IH) with power factor correction (PFC) for domestic induction heating applications. A half bridge voltage fed series resonant inverter (VFSRI) based IH is fed from the front end PFC corrected zeta converter. The PFC-zeta converter operating in continuous inductor conduction mode (CICM) is used to regulate the DC link voltage. The switch current stress of PFC-zeta converter is controlled by operating zeta converter in CICM mode using a well-established internal current loop and outer voltage loop approach. The PFC-zeta converter based voltage fed IH converts intermediate DC bus voltage to high frequency (30 kHz) voltage suitable for domestic induction heating. A 2 kW PFC-zeta converter based IH is designed and its performance is simulated in MATLAB with power quality indices within an IEC 61000-3-2 standard.**

Keywords*— *Zeta converter, power factor correction (PFC), induction heating (IH), voltage fed series resonant inverter (VFSRI), power quality (PQ), total harmonic distortion (THD).

I. INTRODUCTION

High frequency induction heating (IH) has gained significant attention due to its fast, safe, highly efficient and contactless heating. With considerable advancement in semiconductor technology, fast and adaptive digital control, high frequency magnetics technology and noise less heating operation, IH is becoming a preferred heating technology in domestic, industrial process and medical applications. Several topologies of voltage fed series resonant inverters (VFSRIs) have been reported for IH in [1-5]. Depending upon the output power levels, half bridge and full bridge VFSRIs are used to realize IH. These converters have high efficiency due to features like zero voltage switching (ZVS) and require small sized snubbers, thus, achieving a high power density. ZVS operation of VFSRI enables the power electronics engineer to operate the converter at higher switching frequencies, thus reducing the size of magnetics and consequently the converter cost to a great extent. The above mentioned features have enabled the use of VFSRI as a preferred choice for IH.

A conventional VFSRI with a diode bridge rectifier (DBR) and hold-up capacitor at DC bus can provide cost effective and efficient design but such configuration results in a peaky, distorted and harmonic rich current [6] from input supply mains. This leads to poor power factor and high current distortion, violating the international standard limits as stated in IEC-61000-3-2 standard [7]. Thus, the use of improved power quality converters (IPQC) becomes indispensable to comply with international power quality standards.

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Single stage bridgeless boost based single stage AC-AC converter has been proposed in [1]. However, a PFC-boost converter suffers from the drawbacks of high inrush current and no isolation. Single stage ZCS converter for IH was proposed in [2], while more popular soft switched ZVS IH converters have been proposed in [3-5]. At medium power levels, half bridge VFSRI is the obvious choice since it requires lesser switching devices. Various configurations of power factor correction converter topologies based on buck, boost, and buck- boost converters have been investigated in the literature [8-9]. Primarily IPQC may be designed in discontinuous inductor conduction mode (DICM) or continuous inductor conduction mode (CICM). While CICM operation of IPQC provides lower current stresses to the devices with complex control, DCM operation results in a simple control loop structure. Consequently, the choice of mode of operation is adequately justified by the power levels, device ratings and magnetics saturation. The DICM operation also uses an input LC filter to maintain harmonic free current at the input AC mains, but an inappropriate DICM mode design can lead to high ripple current flow through input capacitor filter leading to its deterioration over a period of time. Hence, for power levels in excess of 1kW, CICM operation of IPQC proves to be a better choice than DCM operation. Although, a PFC-boost converter is a well-established low cost topology and choice of many power designers, the boost voltage cannot be less than peak of input AC voltage for its operation. For universal AC mains operation (90V-300V AC input), the steady state boost voltage is 425V. With 100Hz ripple, the instantaneous voltage may well be in excess of 450V which can dry up the hold-up electrolytic boost capacitor over a period of time and in addition provides higher voltage stresses to the second stage VFSRI devices. Considering the above said merits and demerits, a PFC-zeta converter [10] fed VFSRI is proposed for domestic heating applications.

II. PROPOSED PFC-ZETA CONVERTER BASED IH

The system configuration of proposed PFC-zeta converter based IH is shown in Fig. 1. In this configuration, the input AC mains is connected to DBR (Diode Bridge Rectifier) which is followed by zeta converter acting as pre-regulator to achieve unity power factor at input AC mains. The proposed converter is operated in CICM mode by sensing the rectified input AC current thus minimizing the device and magnetics current stresses in comparison to DICM mode of operation. The intermediate DC bus voltage which is the input to the VFSRI-IH is regulated by an outer voltage control loop by sensing the intermediate DC link voltage.

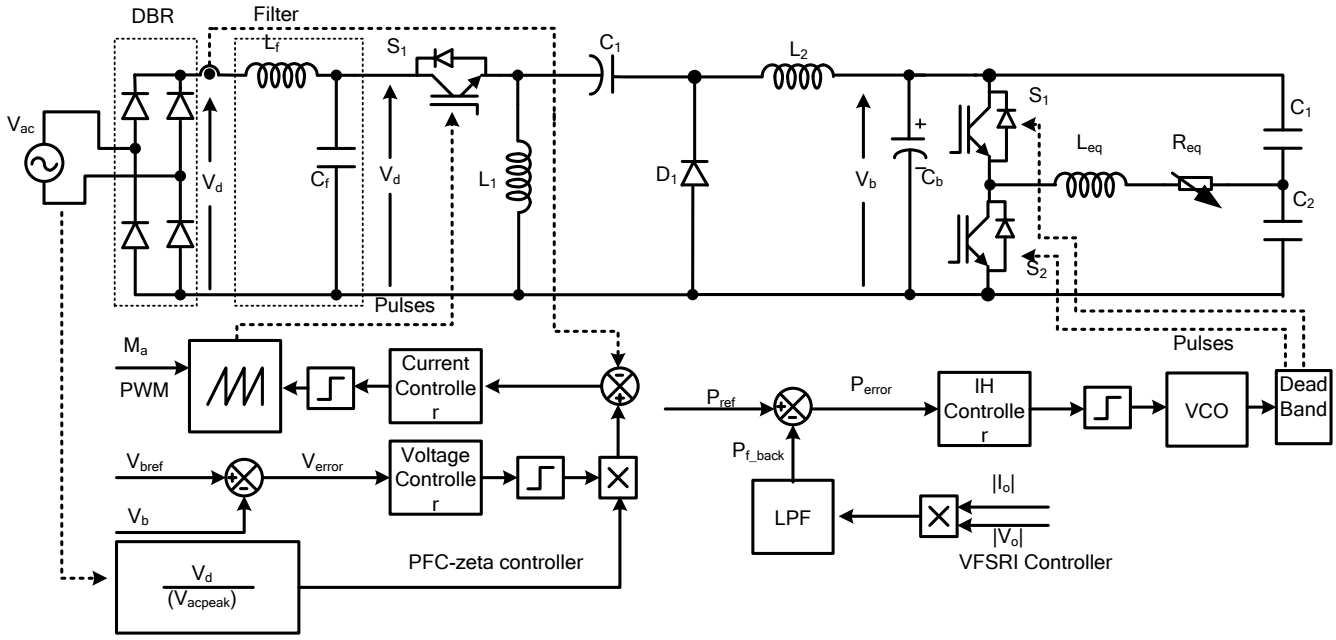

Fig. 1 Configuration of proposed zeta converter fed VFSRI-IH.

This optimizes the operating frequency and limits the device voltage stresses of DC-AC IH converter. The VFSRI-IH converter is operated in pulse frequency mode (PFM) to achieve controlled and good quality induction heating. The proposed PFC-zeta converter is designed to have good dynamic response to tightly regulate the intermediate DC voltage during fast dynamic input voltage variation, thus, alleviating the device voltage stresses on VFSRI-IH.

As shown in Fig. 1, the voltage control loop provides a DC current reference, which is then multiplied by unit voltage template derived from input voltage to generate input reference current. The fast internal current loop ensures that the input current is sinusoidal and harmonics free. The cut off frequency of voltage loop at least a decade smaller than the current loop to ensure there is non-interaction between two loops. The VFSRI-IH control loop senses the voltage and current of the working coil to calculate the power feedback. As shown in Fig. 1, a low pass filter eliminates the higher order harmonics from entering the control loop. The IH controller converts the error to a value which, in turn is converted to an equivalent frequency by a voltage controlled oscillator (VCO). Complimentary gate drives are issued to the IH by providing appropriate dead band to ensure soft switching and to avoid shoot through the VFSRI bridge leg.

III. Operation Of Proposed PFC-ZETA Based VFSRI-IH Converter

This section explains the operating modes of both the converters. Based upon following assumptions, the design and operation of the proposed PFC zeta converter fed VFSRI- IH load is analyzed.

1) Ideal semiconductor devices are considered for analysis.

2) Intermediate boost capacitor is considered to be large enough to avoid any interaction with VFSRI-IH.

3) The input supply voltage V_{ac} is considered to be unchanged during switching period, due to the fact that switching frequency $f_s >> f_{line}$.

A. Operation of PFC-Zeta Converter

The operating conditions of PFC-zeta converter can be divided into two stages for CICM operation. The operating modes during switch on and off time, as shown in Fig. 2-Fig. 4 can be explained as follows.

Stage 1: During stage 1 as shown in Fig. 2, the switch S_1 is on while the zeta converter diode D1 is reversed biased. During this mode, the input inductor L_1 stores energy from the input AC mains and the zeta capacitor C_1 discharges through L_2, thus charging the output inductor. During this mode the intermediate capacitor voltage (V_{C1}) decreases and the DC link voltage (V_b) increases.

Stage 2: This stage is shown in Fig. 3. This stage starts when the main switch S_1 is turned off. During this stage energy stored in inductor L_1 is transferred to intermediate bus capacitor C_1 through forward conduction of diode D_1. The energy stored in inductor L_2 is delivered to intermediate DC link through forward conduction of diode D_1. The switching waveforms during the two modes are shown in Fig. 4.

B. Operation of VFSRI-IH Converter

The regulated DC link output voltage of PFC zeta converter is fed to the second stage VFSRI-IH converter. The modes explaining the operating modes are shown in Fig.5. The operating modes of the VFSRI -IH can be categorized into four stages as follows.

Stage 1: During this stage, the upper switch S_1 is turned on and the energy stored in inductive coil is transferred to load by electromagnetic induction. During this mode, the lower resonant capacitor C_{R2} is charged and upper resonant capacitor C_{R1} is discharged.

Stage 2: This stage starts when the upper switch S_1 is switched off. As soon as the upper switch is switched off, the resonant current free-wheels its energy through the body diode of lower switch d_{S2}, thus enabling it to turn on under ZVS condition.

Stage3: This stage is similar to stage 1. The lower switch S_2 is switched on under ZVS condition and the current through the working induction coil reverses. The energy stored in the working induction coil is transferred to the load by electromagnetic induction and is dissipated in heating load majorly as Joule's heat. During this stage, the upper capacitor C_{R1} is charging while the lower capacitor C_{R2} is discharging.

Stage4: This stage is just the reverse of stage 2. The VFSRI-IH operation continues in push pull fashion.

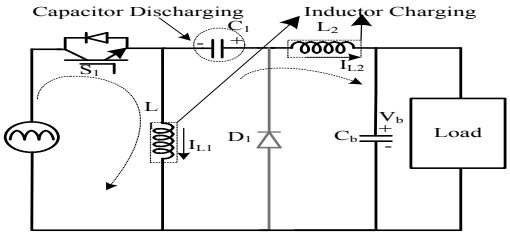

Fig. 2 Stage 1- Operation of PFC-zeta converter during T_{on}.

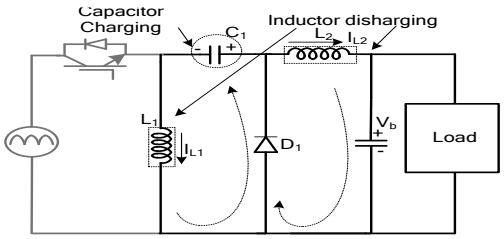

Fig. 3 Operation of PFC-zeta converter during T_{off}.

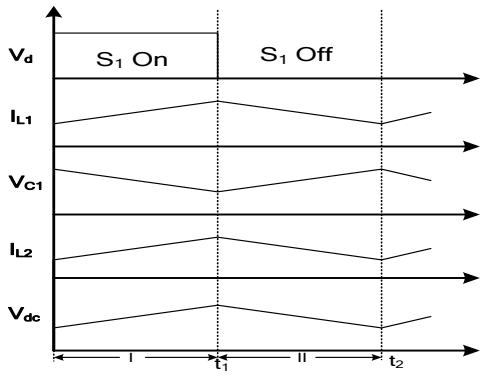

Fig. 4 Switching waveforms of PFC-zeta converter.

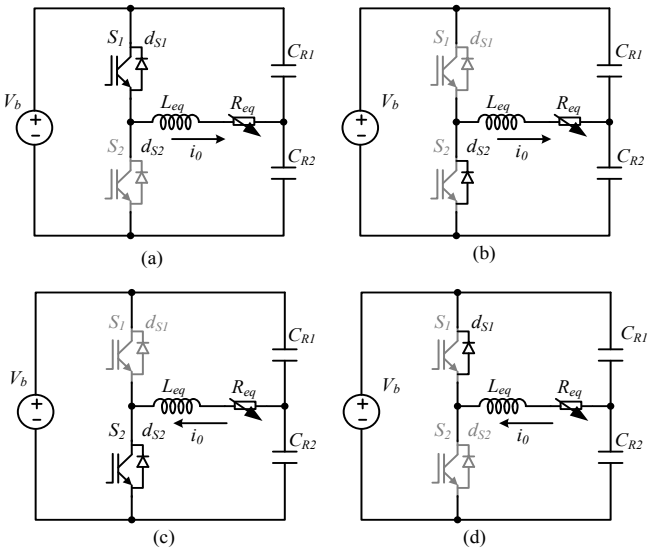

Fig. 5 Operating modes of VFSRI-IH DC-AC inverter.

IV. Design Of Proposed PFC-ZETA Based VFSRI-IH Converter

A 2 kW PFC-zeta converter fed VFSRI-IH is designed, modelled and simulated in MATLAB environment for its feasibility. The design of key components is explained as follows.

A. Design of Input Filter

The input filter capacitance C_f is selected to supress the higher order harmonics from appearing in the input AC line current.

$$C_f = \frac{I_m \tan\theta}{2\times\pi\times f_L \times V_{ac}} = \frac{\left(\frac{\sqrt{2}\times 2000}{185\times 0.96}\right)\tan\left(1^\circ\right)}{2\times\pi\times 50\times\sqrt{2}\times 185} = 3.38\mu F$$

Where I_m and V_m are peak values of ac input line voltage and current and θ is selected to achieve high power factor at input mains with the optimum value of 1°. Assuming a practical efficiency of 96% of LLC-IH dc-ac inverter a 2.20μF capacitor is selected. With the selected value of input filter capacitor and considering 20 kHz switching frequency of buck-boost converter, a 3 kHz cutoff frequency of input LC filter is selected by the following expression,

$$L_f = \frac{1}{4\times\pi^2\times f_c^{\,2}\times C_f} = \frac{1}{4\times\pi^2\times 3000^2\times 2.2\mu} = 1.23mH$$

Based on above equation 1.2mH inductor is selected.

B. Design of PFC-Zeta Converter

The instantaneous value of duty ratio D(t) depends on converter output voltage V_b and the voltage appearing after DBR $V_d(t)$. The expression for D is given as,

$$D(t) = \frac{V_b}{V_b + V_b(t)}$$

In CICM mode the duty cycle varies theoretically from 100% at zero crossing of the line voltage to a minimum value at peak of the minimum rms AC mains voltage. At this point the input inductor is under worst current stress. The duty cycle at maximum current is given as,

$$D_{max}=\frac{V_b}{V_b+\sqrt{2}\times V_{in}}=\frac{350}{350+\sqrt{2}\times 185}=57.22\%$$

Assuming ideal conditions, a coupled inductor approach for practical realization of both inductors on single core is more suitable from economic design point and lower EMI filtering requirements. The inductance requirement in a coupled inductor design is half when compared two separate inductors. A peak to peak ripple current of 40% of the input current is distributed in equal values in L_1 and L_2 and is given as,

$$\Delta I=\frac{\sqrt{2}\times 40\% \times P_0}{\eta\times V_{inmin}}=\frac{\sqrt{2}\times 0.4\times 2000}{1\times 185}=6.12A$$

The input and output inductors can be calculated as,

$$L_1=L_2=\frac{1}{2}\times\frac{\sqrt{2}\times V_{inmin}\times D_{min}}{\Delta I\times f_s}=\frac{\sqrt{2}\times 185\times 0.5722}{6.12}=611\mu H$$

Selecting the input and output inductors to be 610µH, the peak current stresses in input and output inductors is given as,

$$I_{L1peak}=I_{inpeak}+\frac{\Delta I}{2}=15.28+\frac{6.12}{2}=18.34A$$

$$I_{L2peak}=I_{opeak}+\frac{\Delta I}{2}=\frac{2000}{350}+\frac{6.12}{2}=8.75A$$

The coupling capacitor and its current rating are given as,

$$C_1=\frac{V_o\times D_{max}}{R\times f_s\times \Delta V_c}=\frac{2000\times 350\times 0.5722}{350\times 350\times 20000\times(185*1.414+350)}=292nF$$

$$I_{C1rms}=I_o\sqrt{\frac{V_b}{V_{inmin}}}=\frac{2000}{350}\times\sqrt{\frac{350}{1.414\times 185}}=6.6A$$

The DC link capacitor design is given as,

$$C_b=\frac{P_o}{2\times\pi\times f_L\times V_b\times\Delta V_b}=\frac{2083}{2\times\pi\times 100\times 350\times 15}=736\mu F$$

C. Design of VFSRI-IH

The VFSRI-IH design mainly constitutes of the choice of resonant frequency, resonant capacitors, quality factor, damping ratio, equivalent coil inductance and equivalent resistance of the working induction coil and load. Assuming that under maximum loading conditions, the operating frequency of VFSRI equals to the tank resonant frequency, thus, resulting in zero phase displacement between the exciting voltage and resonant current, the equivalent resistance can be expressed as follows,

$$R_{eq}=\frac{2V_b^2\cos^2\varphi}{\pi^2 P_0}=\frac{2\times 350^2\cos^2(0^\circ)}{2000\times\pi^2}=12.42\ \Omega$$

The average DC input current can be expressed as average of resonant current over a switching cycle, thus the peak resonant tank current which also is the peak switch current can be expressed as,

$$I_{res\_Peak}=\frac{2\pi.P_o}{2V_b}=\frac{2\pi.2000}{700}=17.952\ A$$

Selecting the resonant frequency as 30 kHz, the resonant capacitor can be selected as,

$$C_R=\frac{I_{res\_peak}}{2\pi f_r V_b}=\frac{17.952}{2\pi\times 30000\times 350}=272nF$$

This capacitor is split in two equal capacitors C_{R1} and C_{R2} having half the value of C_R to form bridge configuration. The resonant coil inductor can be selected as,

$$L_R=\frac{1}{(2\pi f_r)^2 C_R}=\frac{1}{(2\pi\times 30000)^2\times 264n}=107\mu H$$

The corresponding quality factor and damping ratio at full load can be expressed as a function of the resonant tank elements as,

$$Q=\frac{2\pi f_r L_r}{R_{eq}}=\frac{2\pi\times 30000\times 107u}{12.42}=1.67$$

$$\zeta=\frac{R_{eq}}{2}\sqrt{\frac{C_R}{L_R}}=\frac{12.42}{2}\sqrt{\frac{272n}{107\mu}}=0.32$$

V. Results and Discussion

A 2 kW, PFC-zeta based VFSRI-IH converter is modeled and simulated in MATLAB SIMULINK environment. The controller gains used during simulation are given in Appendix. Simulation results of PFC-zeta fed VFSRI-IH are shown and discussed in the following sections.

A. Steady State Performance

Fig. 6 and Fig. 7 show the performance of proposed converter under steady state condition with nominal line voltage ($220V_{rms}$) and full load of 2 kW. It is observed from Fig. 6 that the PFC zeta converter regulates the intermediate DC link voltage to 350V, while maintaining low THD (Total Harmonic Distortion) of input current. Fig. 6 shows that CICM mode of operation of input inductor can be successfully achieved with the selected magnetics and control strategy. Fig. 7 shows that the VFSRI-IH regulates the output power and achieves high efficiency due to zero voltage switching. Table-I outlines the steady state performance and device stresses of the proposed converter at quarter load, half load and full load.

B. Dynamic Performance Under Line Voltage Variations

Fig. 8 shows the simulated results of proposed converter under dynamic variation of input AC line voltage. The converter is operating at full load and $220V_{rms}$ till 0.4s.

At t=0.4s, the line voltage dips to a minimum value of $185V_{rms}$. It is observed that the magnitude of input current increases to regulate the intermediate bus voltage, while the VFSRI-IH power control loop is fast enough to accommodate for input line disturbance, causing very little effect on power delivered by IH. At t=0.6s, the line voltage is increased to a maximum value of $265V_{rms}$ from a minimum of $185V_{rms}$. It is observed that even in this extreme voltage transient, the input current changes fast enough to regulate the intermediate bus voltage, while the VFSRI-IH power control loop is fast enough to accommodate for input line disturbance, resulting feeble effect on output power delivered to load. The voltage restores to normal value at t=0.7s.

D. Dynamic Performance of Converter Under the Load Variations

Fig. 10 shows the simulated results of proposed improved power quality converter under dynamic load variations at $220V_{rms}$. As shown in the results at t=0.4s, the load is reduced 1.0 kW from 2 kW and load is restored from 1 kW to 2 kW at t=0.6s. Both PFC-zeta converter and VFSRI-IH converters counter to this load change by adjusting their respective currents, thus regulating the power delivered to the IH. Fig. 11 shows the AC input current harmonics under nominal input AC voltage at full load. It is observed that the input AC current THD (Total Harmonic Distortion) is 0.81% and it is in accordance with IEEE-61000-3-2 standard.

VI. CONCLUSIONS

A 2 kW PFC zeta converter fed VFSRI-IH has been modeled, designed and simulated in MATLAB/Simulink sim power systems (SPS) toolboxes. A dual loop structure for PFC zeta converter and power loop structure for VFSRI-IH have been designed and tested using MATLAB for its practical implementation. The design methodology for magnetics and capacitors under CICM has led to lower device current stress, and prevents saturation of magnetics. The CICM mode of operation has led to lower current rating device selection for PFC converter. The ripple steering by use of coupled inductor has led to lower EMI requirements at input stage and requires less inductance value. PFC zeta converter topology has enabled the designer to use lower voltage rating devices in DC-AC inverter stage, thus, providing an economical design at higher power ratings.

The steady state and the dynamic state performance of the proposed converter depict the efficiency and ability of control loop to regulate the output power while maintaining good power quality at input AC mains.

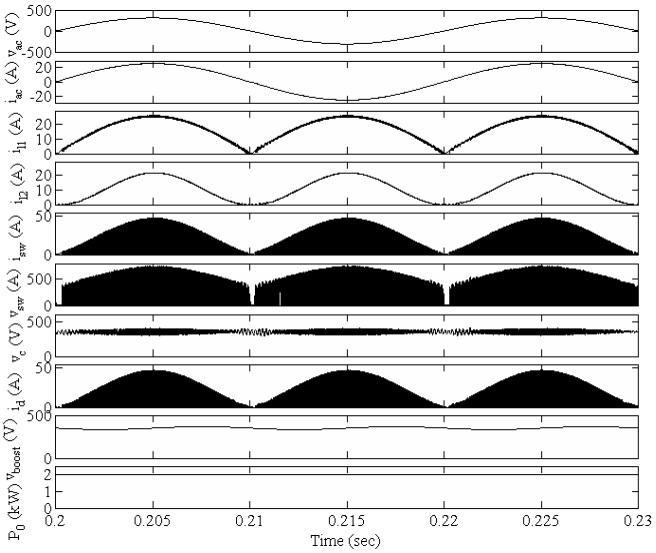

Fig. 6. Steady state waveforms of proposed converter at 220 V (rms), waveforms of v_{ac} , i_{ac} , i_{l1} , i_{l2} , i_{sw} , v_{sw} , v_c , i_d , v_b , P_o.

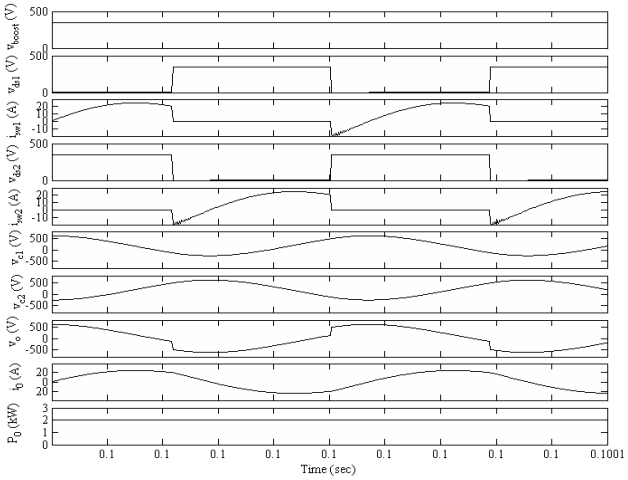

Fig. 7. Steady state waveforms of VFSRI-IH converter at 350 V_{dc} input, waveforms of v_b , v_{ds1} , i_{sw1} , v_{ds2} , i_{sw2} , v_{c1} , v_{c2} , v_o , i_o , P_o .

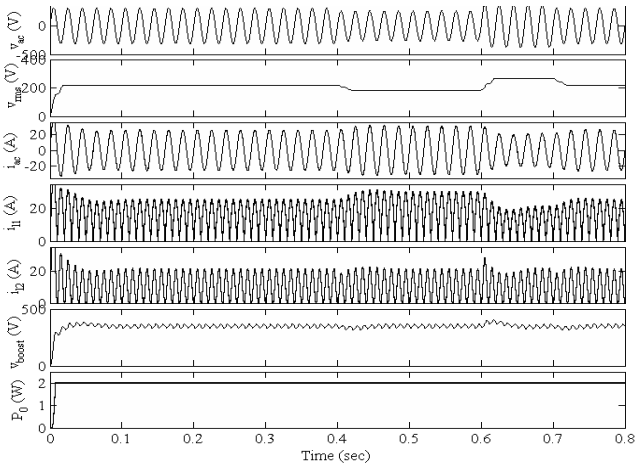

Fig. 8. Dynamic performance of the proposed converter during line voltage variation from $220V_{rms}$ - $185V_{rms}$ - $265V_{rms}$ - $220V_{rms}$, waveforms of waveforms of v_{ac} , v_{rms} , i_{ac} , i_{l1} , i_{l2} ,v_b , P_o .

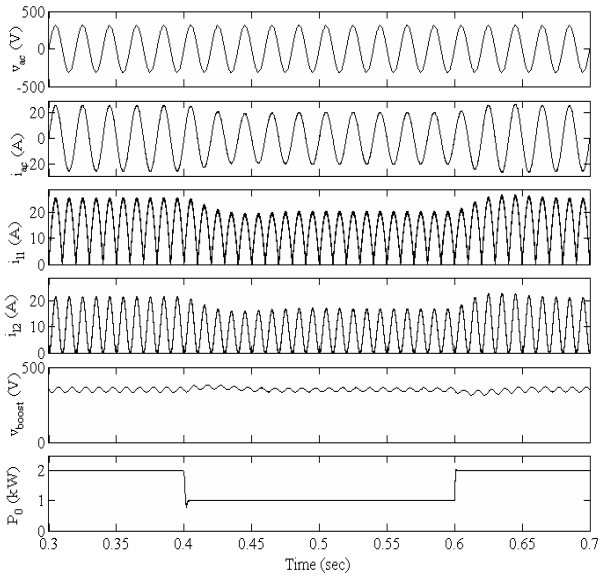

Fig. 9. Dynamic performance of the proposed converter during load variation from 2kW-1kW-2kW, waveforms of v_{ac} , i_{ac} , i_{l1} , i_{l2} ,v_b , P_o.

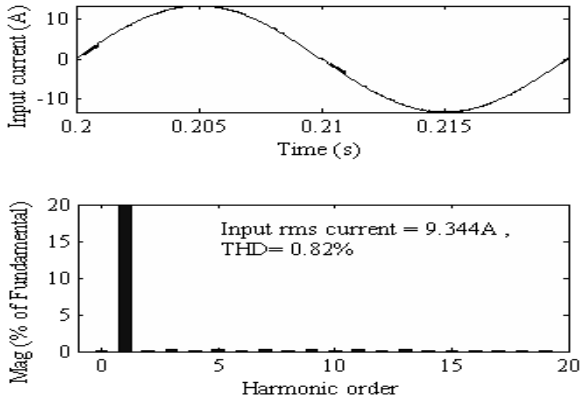

Fig. 10. PQ indices of proposed converter at 2 kW load and 220Vrms input AC voltage.

Appendix

PFC-zeta voltage controller gains: K_p=0.06, K_i=3; PFC-zeta current controller gains: K_p=0.01, K_i=60; VFSRI-IH controller gains: K_p=0.5, K_i=2.

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TABLE I
PERFORMANCE OF PROPOSED CONVETER AT VARYING VOLTAGES AND LOAD

V_{rms}(V)	I_{rms}(A)	V_{sw_pk} (V)	$I_{sw\,pk}$ (A)	P_o (kW)	THD_i (%)	DPF	DF	PF
220	9.344	700	25.5	2	0.82	1	1	1
185	11.17	652	28	2	0.52	1	1	1
265	7.768	765	23.5	2	0.50	1	1	1
220	4.702	684	12.5	1	0.48	1	1	1
185	5.578	635	14.5	1	0.65	1	1	1
265	3.919	748	12	1	0.46	0.9999	1	0.9999
220	2.427	672	7.2	0.5	0.70	0.9999	1	0.9999
185	2.82	626	7.4	0.5	0.66	0.9999	1	0.9999