Abstract—A major drawback in case of three-level PWM rectifiers is unbalance in DC-bus capacitor voltage which is further aggravated under unbalanced load conditions. The DC-bus capacitor voltage unbalancing is created due to irregular charging and discharging of the capacitors which is originated by asymmetric connections produced by power semiconductor devices in the converter. The capacitor voltage unbalancing has become a burning issue and has invited an intensive research to address this problem in multilevel inverters. The key aspect in the behavior of multilevel rectifiers is to avoid the unbalance in DC-bus capacitor voltages.

In the proposed work, a linear controller is used to control the total DC-bus voltage in a similar fashion as in two-level PWM rectifiers. A non-linear controller is proposed to achieve the balancing of the DC-bus capacitor voltages. In fact, the mechanism which generates the DC-bus capacitor voltage unbalancing is studied and is used to develop the proposed control algorithm. The redundant switching vectors are used for achieving the capacitor voltage balancing. The proposed control algorithm is referred to as voltage balancing strategy.

Keywords—Power electronic converter, nonlinear load, voltage balancing, DC bus capacitor, performance evaluation etc.

I. INTRODUCTION

In recent years, the popularity of medium voltage converters has grown and this has invited the attention of industry [1, 2, 3, 4, 5]. Among the various types of PWM converters, the three-level three-phase neutral-point clamped (NPC) converter has received special attention because of its various attractive features mainly due to series power switches connection. Each power switch is stressed to half the DC-bus voltage instead of full DC-bus voltage. The DC-bus capacitor voltage unbalancing in case of three-level PWM rectifiers is further aggravated under unbalanced load conditions. The DC-bus capacitor voltage unbalancing is created due to irregular charging and discharging of the capacitors which is originated by asymmetric connections produced by power semiconductor devices in the converter. The capacitor voltage unbalancing has become a burning issue and has invited an intensive research to address this problem in multilevel inverters [6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17]. The key aspect in the behaviour of multilevel rectifiers is to avoid the unbalance in DC-bus capacitor voltages. In [9], the authors proposed a solution to overcome this problem by controlling the neutral branch current.

II. PROPOSED CONTROL STRATEGY

As shown in the power circuit of the three-phase neutral-point clamped rectifier of Fig. 1, the input terminals a, b, and c are connected to the terminals of three-phase source A, B, and C, through the boost inductance L. The power switches of the rectifier are commutated with a high switching frequency to generate the PWM voltages \( v_a \), \( v_b \), and \( v_c \) on the rectifier input terminals.

Considering the definitions of space vectors, we have:

\[
v = \frac{2}{3}(v_a + a_v + i^3_v)
\]

\[
v' = \frac{2}{3}(v_a' + a_v' + i^3_v')
\]

\[
i = \frac{2}{3}(i_a + a_i + i^3_i)
\]

The voltage vector equation can be written as:

\[
v = L \frac{di}{dt} + v'
\]

The above equation can be expressed in the rotating frame of reference \((d-q)\), with the \(d\) -axis oriented in the direction of source voltage vector \(v\). In this way, equation (4) can be written in the form of the following equations:

\[
v_d = L \frac{di_d}{dt} + \omega L i_q + v_d'
\]

\[
v_q = 0 = L \frac{di_q}{dt} + \omega L i_d + v_q'
\]

where \(\omega\) is the angular frequency of the three-phase voltage, \(v_d\), \(v_d'\), \(i_d\) and \(v_q\), \(v_q'\), \(i_q\) are the components of \(v\), \(v'\) and \(i\) in the \(d\)-axis and \(q\)-axis, respectively.
The space vector modulation principle is used for the modulation of this rectifier. Applying the definition of equation (2) to all the 27 possible conduction states of the power semiconducting devices, the rectifier generates 19 different vectors. This figure also shows the commutation states used to generate each vector. These 19 vectors divide the entire complex plane into 24 triangles, called regions, and six sectors with four regions in each sector. Fig. 2(b) shows the reference rotating vector \( V' \) in the complex (\( \alpha - \beta \) ) plane. This reference vector is obtained from the voltage and current control loops of the rectifier. Assuming the reference vector to be located in region \( R_1 \), the rectifier generates vectors \( V_1, \ V_6 \) and \( V_2 \) during the time intervals \( T_a, \ T_b \) and \( T_c \) respectively. These vectors are used to generate the desired voltage vector in terminals \( a, b \) and \( c \) according to the following equations:

\[
V_{iT_a} = V_1 T_a + V_2 T_c = V' T_s / 2 \quad (7)
\]

\[
T_a + T_b + T_c = T_s / 2 \quad (8)
\]

Where \( T_a, T_b, \) and \( T_c \) are the respective vector time intervals and \( T_s \) is the modulation period. The modulator calculates the values of \( T_a, T_b, \) and \( T_c \) necessary to accomplish equations (7) and (8). The modulator also defines which commutation state of the rectifier corresponds to \( V_1, \ V_6 \) and \( V_2 \), depending on the position of the reference vector \( V' \).

\[i_0 = i_{n1} - i_{n2}\]  

For zero neutral current, \( i_0 = i_{n1} \) and the capacitor voltages remain balanced.

\[i_0 = i_{n1} \quad (9)\]

A. Causes of Capacitor Voltage Unbalance

It is assumed that \( C_1 = C_2 \) and initially \( V_{c1} = V_{c2} \). A DC-bus capacitor voltage unbalance will occur only when the capacitor currents \( i_{c1} \) and \( i_{c2} \) are different. The neutral current \( i_0 \) is defined by:

\[i_0 = i_{c1} - i_{c2}\]  

From Fig. 3, the commutation state \( V_{c1}^+ \) produces:

\[i_0 = i_{c1}\]  

(10)
And the commutation state $V_i^+$ produces,

$$i_o = -i_a$$  \hspace{1cm} (11)

**B. Relation between Direction of Power Flow and Capacitor Voltage Unbalance**

The direction of power flow between the source and converter changes the polarity of DC-bus capacitor voltage unbalance ($\Delta V = V_{c1} - V_{c2}$). This can be clearly observed from Fig. 3. If the three-phase source delivers active power to the rectifier in commutation state $V_i^+$, this power is received by the capacitor $C_1$ resulting in an increase in $V_{c1}$. The voltage control loop acts to keep the total DC-bus voltage $V_0$ constant. It means that in this condition the voltage across capacitor $C_2$ (i.e. $V_{c2}$) will reduce in order to keep $V_0$ constant. On the other hand, if the rectifier in conduction state $V_i^-$ works in the inversion mode to regenerate the active power to three-phase AC source, this power will be delivered by capacitor $C_1$, thus causing a reduction in its voltage $V_{c1}$ and a proportional increase in $V_{c2}$.

Now if the three-phase source delivers active power to the converter in the commutation state $V_i^-$, this power is received by the capacitor $C_2$, thus causing an increase in $V_{c2}$ and a decrease in $V_{c1}$. On the other hand, if the rectifier in state $V_i^-$ delivers active power to the three-phase source, this power comes from $C_2$, thus resulting in a reduction of $V_{c2}$ and an increase in $V_{c1}$. This analysis is valid for all the internal vectors.

**C. Voltage Balancing Strategy**

The difference in the capacitor voltages is defined by the following equation:

$$\Delta V = V_{c1} - V_{c2}$$  \hspace{1cm} (12)

It is to be emphasized that the direction of power flow between the converter and AC source is contained in the polarity of the current $i_d^*$. This current in turn follows the reference current $i_d^*$, thanks to the action of the corresponding current controller. Since the actual current $i_d$ has more ripples than the reference current $i_d^*$, it is advantageous to use $i_d^*$ for determining the direction of power flow.

In the control algorithm, according to the information about the polarity of $\Delta V$ and $i_d^*$ in each modulation period $T_s$, the reference vector $V^*$ is generated by using the redundant states of the internal vectors. Considering Fig. 3, if $\Delta V > 0$ meaning that $V_{c1} > V_{c2}$, consequently $V_{c2}$ must increase and $V_{c1}$ must be proportionately reduced to compensate the unbalance. In this situation, if the power flows from the source to rectifier ($i_d^* > 0$), a negative redundant state, like $V_i^-$, must be selected for the internal vectors. On the other hand, if the power flows from the rectifier to source ($i_d^* < 0$), it must be delivered by the capacitor $C_1$ in order to produce a reduction in $V_{c1}$ and a proportionate increase in $V_{c2}$. For this reason, a positive redundant state, like $V_i^+$, must be chosen for the internal vectors.

A similar explanation holds good for the case of $\Delta V < 0$ for both rectification and inversion modes of operation of the converter.

Thus the modified SVPWM control algorithm designed for choosing an appropriate redundant switching state to balance the DC-bus capacitor voltages can be summarized as follows:

- If $\Delta V$ is positive & $i_d^*$ is positive, select a negative redundant state, otherwise select a positive redundant state for negative $i_d^*$.

- If $\Delta V$ is negative & $i_d^*$ is positive, select a positive redundant state, otherwise select a negative redundant state for negative $i_d^*$.

**III. PERFORMANCE EVALUATION OF NPC BIDIRECTIONAL RECTIFIER FOR DC BUS CAPACITOR VOLTAGE BALANCING**

**A. Performance under ideal mains**

The supply main is assumed to be ideal and balanced and the performance of the rectifier is evaluated with these assumptions.

- **a) Operation with balanced load**

![Graph](image)

Fig. 4 Unbalanced DC-bus capacitor voltages

- **b) Phase- a voltage waveform**

![Graph](image)

Fig. 5 (a) Phase- a voltage waveform

- **c) Phase- a current waveform**

![Graph](image)

Fig. 5 (b) Phase- a current waveform

**Fig. 6 Frequency spectrum of source current**
Fig. 7 DC-bus capacitor voltages with voltage balancing strategy

Fig. 8 DC-bus capacitor voltage unbalance ($\Delta V_c = V_{c1} - V_{c2}$) with voltage balancing strategy

Fig. 9 (a) Phase-a voltage and current waveforms in rectification mode with voltage balancing strategy

Fig. 9 (b) Rectifier input voltage $V_{ab}$

Fig. 10 Frequency spectrum of phase-a source current

Fig. 11 Phase-a voltage and line-current waveforms in inversion mode with voltage balancing

Fig. 12 Frequency spectrum of source current in inversion mode

Fig. 13 Load voltage waveform

Fig. 14 DC-bus capacitor voltages before and after applying voltage balancing strategy

Fig. 15 (a) Load voltage waveform for sudden decrease in load (with voltage balancing strategy)

Fig. 15 (b) Source voltage and source current waveform for sudden decrease in load

Fig. 16 (a) Load voltage waveform for sudden increase in load (with voltage balancing strategy)

Fig. 16 (b) Source voltage and source current waveform for sudden increase in load

Fig. 17 (a) Phase-a voltage and current waveforms for a decrease in mains voltage

Fig. 17 (b) Phase-a voltage and current waveforms for an increase in mains voltage

b) Operation with unbalanced load
In order to analyze the performance under non-ideal mains conditions, the mains voltage can be represented as:

\[
\begin{bmatrix}
    v_a \\
    v_b \\
    v_c
\end{bmatrix}
= \begin{bmatrix}
    v_{a1} \\
    v_{b1} \\
    v_{c1}
\end{bmatrix} + \begin{bmatrix}
    v_{ah} \\
    v_{bh} \\
    v_{ch}
\end{bmatrix}
\]  

(13)

where \(v_{a1}, v_{b1}, v_{c1}\) are the three-phase fundamental components of mains voltage and \(v_{ah}, v_{bh}, v_{ch}\) are the harmonic components of mains voltage.

\[
v_a = 165\sin(\omega t) + 20\sin(5\omega t) \\
v_b = 165\sin(\omega t - 120^\circ) + 20\sin(5\omega t - 120^\circ) \\
v_c = 165\sin(\omega t + 120^\circ) + 20\sin(5\omega t + 120^\circ)
\]  

(14)
IV. CONCLUSIONS

In this paper, a voltage balancing algorithm (modified space vector modulation) is proposed for perfect balancing of the capacitor voltages. The mechanism responsible for producing the unbalance in capacitor voltages is then studied. The redundant switching states of internal space vectors are used for balancing the capacitor voltages. Based on the polarity of capacitor voltage difference and direction of power flow, a suitable switching vector is selected. The proposed control algorithm is capable of balancing the capacitor voltages under different operating conditions like rectification and inversion modes, sudden load changes, and fluctuations in the supply voltage. If the conventional SVM-based rectifier is operated under unbalanced load conditions, the current tends to flow in the DC-bus neutral. Hence the irregular charging and discharging of capacitors due to unbalanced load conditions causes a wide variation in the capacitor voltages which results in the already mentioned problems. In the present paper, the proposed voltage balancing algorithm takes care of this problem and elegantly addresses the capacitor voltage unbalance problem under unbalanced load condition. Simulation results show a highly satisfactory performance of the rectifier with the proposed control algorithm. The rectifier draws sinusoidal currents from the supply with negligible THD and unity input power factor. The DC-bus capacitor voltage unbalance is reduced to less than one volt which is a great achievement.

The performance of the rectifier with proposed control algorithm is evaluated with distorted mains. It is found that the rectifier is capable of restricting the harmonic pollution in supply currents from going to dangerously higher values under distorted mains condition. The simulation results show that the rectifier still draws a sinusoidal current with a THD below 5% recommended limit when fed from a source with a well-defined and predominant 5th harmonic component.

REFERENCES