Analysis and Design of an Active Power Filter using Sliding Mode Control

R.Mahanty, M.P.Kavuri and A.K.Kapoor

Abstract—This paper presents active power filter for single phase nonlinear loads. The active filter is based on a single phase inverter with four controlled switches. The ac side of the inverter is connected in parallel to nonlinear load though an inductance. The inverter switches are controlled to shape the current through the inductor such that the line current is in phase with, and of the same shape as the input voltage. The controller is based on a conceptually simple sliding mode controller. The paper provides background on the operation of the filter, the details of the power circuit and control design.

Index Terms—Active filter, sliding mode control.

I. INTRODUCTION

Over the years there has been a continuous proliferation of nonlinear loads due to intensive use of power electronic control in industry as well as by domestic consumers of electrical energy. As a result, the utility supplying these loads has to supply large reactive volt-amperes, and also the harmonics generated by the load pollutes it. The tariffs charged by utilities against excessive vars and stricter harmonic standards have led to extensive research in this area. The basic requirements for compensation process involve precise and continuous reactive volt-ampere control with fast response time and online elimination of load harmonics. To satisfy these criteria, the traditional methods of reactive volt-ampere compensation using switched capacitor and thyristor controlled inductor coupled with passive filters are increasingly replaced by active filters. Out of the different topologies of active filters, the shunt active filter is the most common topology. It injects equal compensating current, opposite in phase, to cancel harmonics and/or reactive components of the nonlinear load at the point of connection.

Fig.1 shows the basic block diagram of a shunt active filter scheme. It has two control loops viz., voltage control loop and current control loop. The voltage control loop generates the magnitude of the source current reference (k) through a PI controller, which regulates the average value of the capacitor voltage (Vc). The average capacitor voltage is obtained using a low pass filter, which is compared with a reference dc voltage (Vref) and the error is fed to a PI controller. The output of the PI controller is the amplitude (k) of the current, which is used to derive the reference current waveform.

Assume \( |v_s| \geq |v_f| \). During the positive half cycle of the source voltage, \( v_s \), current \( i_L \) can be made positive by making \( v_f = 0 \);
i_c can be driven toward zero by making \( v_s = -v_c \). From this heuristic understanding of circuit operation, it can be concluded that two legs of inverter can be used for different tasks. Switches \( S_3 \) and \( S_4 \) can be used to force \( 0 \leq i_c \) and \( 0 \geq i_c \), respectively, while switches \( S_1 \) and \( S_2 \) are used to actively shape \( i_L \).

\[
\text{Fig. 2. The single phase inverter used as an active filter}
\]

For modeling and control purposes, the state of each inverter is summarised by a switching function such that

\[
u_s = \begin{cases} 1 & \text{when } S_i \text{ is conducting} \\ 0 & \text{when } S_i \text{ is open} \end{cases}
\]  

(1)

Where \( x \) denotes the switch number. Two switches, which comprise each inverter leg, must operate in a complementary fashion. That is one switch must be conducting all the time and both switches are prohibited from conducting at the same time. This gives,

\[
u_1 + \nu_2 = 1
\]  

(2)

and

\[
u_3 + \nu_4 = 1
\]  

(3)

Given the definition of \( \nu \) for each switch, it can be seen that

\[
v_s = \left[ u_1 u_4 - u_2 u_3 \right] v_c
\]  

(4)

using equations (2), (3) and (4)

\[
v_s = \left[ u_1 + u_4 - 1 \right] v_c
\]  

(5)

Further,

\[
i_c = \left[ u_1 + u_4 - 1 \right] i_L
\]  

(6)

From analytical expressions of \( v_s \) and \( i_c \), state equations for the inductor current and capacitor voltage is written as,

\[
i_L = \frac{1}{L} \left[ v_s - \left[ u_1 + u_4 - 1 \right] v_c \right]
\]  

(7)

\[
v_c = \frac{1}{C} \left[ u_1 + u_4 - 1 \right] i_L
\]  

(8)

Sliding mode control is concerned with forcing one or more variables (often, but not necessarily, state variables) to follow a specific trajectory [5]. The trajectory is known as the sliding surface. The location of the variables relative to the sliding surface governs the control law, which is applied to the sliding surface. A nonlinear control law is chosen so that regardless of where the system is with respect to the sliding surface, control action always drives the system towards the sliding surface. Power electronic systems are natural candidates for sliding–mode control because the topology of the circuit changes with the operation of the switches. This varying structure of the system leads to the nonlinear control law which forces the system back to the sliding surface.

The starting point with sliding mode control is the definition of the sliding surface. For the active filter application, the source current is forced to follow the shape and phase of the source voltage. Therefore, the trajectory of the line current is defined as,

\[
i_{ref} = k v_s
\]  

(9)

Where, \( k \) is a scaling factor based on the real power demand of the load. Written in standard form of sliding surface \( s \), we have

\[
s = i_s - k v_s = 0
\]  

(10)

To assure that the system can be maintained on the sliding surface, it must be shown that there is a natural control, which satisfies

\[
s s \leq 0
\]  

(11)

From equation (11), if the sign of \( \dot{s} \) can be controlled, then equation (11) can be satisfied all the time. From equation (10) it can be concluded that controlling the sign of \( \dot{s} \) reduces to controlling the sign of \( i_s \). At any point of time, the filter can force \( i_s \) to be positive and negative through proper operation of the switches. In addition, proper design of the power circuit ensures that \( \left| i_s \right| \cdot \left| k v_s \right| \). From the discussion given in this section, control over \( \dot{s} \) can be accomplished with the nonlinear control law described in table 1.

<table>
<thead>
<tr>
<th>( i_s \leq k v_s )</th>
<th>( i_s &gt; k v_s )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( u_1 )</td>
<td>0</td>
</tr>
<tr>
<td>( u_2 )</td>
<td>1</td>
</tr>
<tr>
<td>( v_s \leq 0 )</td>
<td>( v_s &gt; 0 )</td>
</tr>
<tr>
<td>( u_3 )</td>
<td>1</td>
</tr>
<tr>
<td>( u_4 )</td>
<td>0</td>
</tr>
</tbody>
</table>

**Equivalent control**

The equivalent control concept comes from sliding mode...
control. It is analogous to the continuous-time duty-ratio concept used frequently for the analysis of dc-dc converters. The equivalent control is found by forcing $\dot{s}$ for all time, hereby identically satisfying the requirement for perfect tracking of the sliding surface.

From Kirchoff’s current law at the source,

$$i_s = i_L + i_{Load}$$  \hspace{1cm} (12)

Where $i_{Load}$ is the combined current of the nonlinear load.

From equation (10),

$$\dot{s} = i_s - k\dot{v}_s$$

Substituting (10) and (12) gives,

$$i_{Load} + \frac{1}{L}[v_s + \frac{1}{L}[u_1 + u_4 - 1]v_c - k\dot{v}_s] = 0$$  \hspace{1cm} (14)

Taking the control law for $u_4$ to be as given in Table1,

$$u_4 = \frac{1 + \text{sgn}(v_c)}{2}$$  \hspace{1cm} (15)

where,

$$\text{sgn}(x) = \begin{cases} 1 & \text{for } x > 0 \\ -1 & \text{for } x < 0 \end{cases}$$

Equation (16) can be verified through use of equation (1) and table1. Substituting equation (15) into equation (14) and solving for $u_1$ gives the equivalent control for $S_1$ to be

$$u_{eq} = \frac{L}{v_c} \left[ i_{Load} - k\dot{v}_s \right] + \frac{v_c}{v_c} + \frac{1 + \text{sgn}(v_c)}{2}$$  \hspace{1cm} (17)

Design of filter inductor $L$

There is a fundamental compromise in the selection of $L$. The ability to track the desired source current improves, as the filter inductance is made smaller. As the inductor is made smaller, switching operations must be made during each line cycle in order to keep the ripple in the line current acceptable. A practical choice of $L$ would push $u_{eq}$ close to 1 in order to make the complete use of capacitor voltage.

analog and digital modeling which is suitable to model different control circuits and devices according to the specific requirements. The proposed circuit is simulated for single phase full wave diode rectifier with RC load. The circuit parameters used in simulation are summarised below.

- $R_{load} = 25\Omega$, $C_{load} = 1000\mu\text{f}$
- Filter inductance, $L_f = 5\text{mh}$
- Source inductance, $L_s = 2\text{mh}$
- DC capacitor voltage, $C_7 = 3000\mu\text{f}$
- Switches (S1-S4), IRGBC40F (IGBTs), 600V, 49A, 20kHz
- Diodes (D5-D7), MUR1560, 600V, 30A, $t_{rr} = 65\text{ns}$.

The dc bus capacitor voltage is maintained at 550V by closed loop control. The simulation circuit for the active filter with voltage control loop HB1 and current control loop HB2 is shown in fig. 4. The voltage control loop maintains the capacitor voltage whereas, the current control loop generates the necessary switching pulses for the IGBT switches. The constants for the PI controller are suitable chosen. In the present work $K_p = 37$ and $K_i = 600$. The detailed circuit of blocks HB1 is shown in fig.4. The controller for the sliding mode controller (HB2) is shown in fig. 5. The circuit shows D flip flop labeled $U_7A$. The purpose of this D flip flop is to sample the output of the comparator at the rate decided by the decision clock frequency. The clock input to the flip flop is obtained using a digital clock. The digital output at $Q$ and $\bar{Q}$ pins of D flip flop is brought to analog level of +12V and −2V using comparator. The output of the D flip flop is used to provide gate pulses to the IGBT’s. The output of the current control block gives gating pulses to switches S1 and S2 in accordance to table1. The other two switches S3 and S4 are turned ON and OFF using two pulsed voltage sources, which give gating pulses to S3 and S4 depending on whether the supply voltage is positive or negative.

Simulated waveforms showing the initial settling time of the reference source current are shown in fig. 7.

![Fig. 3 Illustration of switching function $u_1$ and its average $u_{eq}$](image)

**III. CIRCUIT SIMULATION**

The simulation is carried out on the Pspice simulation package MICRISIM 7.1. The package has latest features like...
Fig. 4 Simulation circuit of the active filter

Fig. 5 Voltage control loop of the active filter

Fig. 6 Current control loop of the active filter

Fig. 7 Simulated results (R_{eq}=25\Omega)

IV. CONCLUSION

Several active filter schemes have been reported in the literature for reactive power compensation and reducing the voltage and current harmonics injected into the utility by nonlinear loads. In the present work active filter has been used to supply the reactive power and harmonic demand of the nonlinear load using a sliding mode controller for overall power quality improvement. Without the active filter, the THD in current was 87.8%. However, after connecting the active filter, THD in voltage and current at the point of point of common coupling reduced to less than 5%.

V. REFERENCES

