A High Power Parallel Converter Topology for Load Harmonic and Reactive Power Compensation

Malabika Basu, S. P. Das, Gopal K. Dubey and M. S. Balaji

Abstract—High switching frequency operation in high power is not suitable for the semiconductor switches till date, because of tail current problem, and large switching power loss. To extract superior performance, a combination of high power low switching frequency devices, and low power high switching frequency devices has been proposed in a parallel converter scheme for load compensation suitable for high power application. The VAR of the load is supplied by a high power three level Neutral point clamped (NPC) converter, and the harmonics of the NPC converter and the load are eliminated by a low power current controlled VSI, which is having a common dc link with the NPC converter. As the NPC converter carries the reactive power of the load, it operates at fundamental power frequency and the power capabilities of the switching devices are fully utilized. The current controlled VSI that is connected in parallel with the NPC converter has to handle less power (only harmonics); therefore high switching frequency operation is feasible. The control scheme required for the compensator has been developed. The operation of the scheme is validated through extensive simulation studies in SABER simulator. The overall system has got good dynamic response.

Index Terms—Custom power, power quality issues.

I. INTRODUCTION

With rapid progress in semiconductor technology, active solution to VAR compensation and harmonic elimination of loads are preferred to passive filter solutions, due to availability of fast acting switching devices having moderate power rating. But, long tail current associated with the device characteristics prohibits high switching frequency operation at high power. Also, at high power, the efficiency of Active Power Filters (APF) is less due to significant switching loss. To attend this problem, a new technique to combine high power low frequency devices and low power high frequency devices has been reported for superior performance in VAR compensation [1, 2]. A high power converter (main converter), which consists of high power low switching frequency devices, is operated at low frequency to deliver the VAR requirement of the load. Another converter (auxiliary converter), which consists of low power high frequency devices, is operated in parallel to it. The auxiliary converter eliminates the harmonics produced by the main converter such that the utility current THD is less than 5% (as specified in IEEE-519), and its power rating is low (as it does not handle the reactive load current). The main converter reported in [1, 2] is a voltage source inverter (VSI), which is controlled in selective harmonic elimination technique such that a few lower order harmonics are eliminated with moderate PWM switching frequency (400 Hz).

To lower the switching frequency of the main converter further to fundamental power frequency (50 Hz), a new combination of power circuit topology has been investigated and reported in this paper along with a control technique. Attempts have been focused on the effectiveness of a three level Neutral Point Clamped (NPC) inverter [4, 5], which can be rated for high power (main converter), as one of the parallel converters, with a dedicated task of VAR compensation of load at fundamental power frequency.

With the increase in level of voltage in the multilevel converter, the converter-produced harmonics would have reduced, but the number of components of the converter would have increased [6], and control would have been more complex. Instead, the three level NPC converter is operated in parallel with a current controlled VSI of low power high switching frequency capability, to take care of the harmonics produced by the main converter with reduced control complexity. If the load also produces harmonics, that too can be eliminated by the auxiliary converter. Thus by dedicated task sharing, the efficiency of the parallel load compensation scheme is maximized.

To show the usefulness of the proposed control scheme, an extensive simulation study has been carried out using

1. M. Basu is with the Department of Electrical Engineering, Jadavpur University, India (email: mbasu_b@yahoo.co.in)
2. S. P. Das is with the Department of Electrical Engineering, Indian Institute of Technology, Kanpur, India (email: spdas@iitk.ac.in)
3. G. K. Dubey is with the Department of Electrical Engineering, Indian Institute of Technology, Kanpur, India (email: gkdubey@iitk.ac.in)
4. M. S. Balaji is with the Department of Electrical Engineering, Indian Institute of Technology, Kanpur, India (email: balaji@iitk.ac.in)
SABER simulator. The results show good transient and steady state response of the proposed system.

II. POWER CIRCUIT CONFIGURATION

Fig. 1 describes the power circuit configuration of the proposed scheme. A three phase three wire star connected utility is considered. The combined APF is connected in parallel to the load.

The main converter is a neutral point clamped three-level inverter, with high power low frequency devices (like GTO). The switching loss is minimized and the full utilization of the switching devices’ power capability is realized by keeping the switching frequency to fundamental power frequency only.

The auxiliary converter consists of low power high frequency devices (like IGBT), controlled by current controlled modulation technique. The two converters share the same dc link capacitor leading to a compact structure. The auxiliary converter is connected in parallel to the load as well as main converter through an isolation transformer. This prevents the circulating reactive current between the two converters even though they share the common dc link.

It is essential to ensure that the two capacitors are charged to same voltage because unequal voltage will generate even harmonics. A simple chopper circuit has been used to maintain the charge balanced between two capacitors.

III. CONTROL STRATEGY

The load under study is a phase-controlled rectifier, which simultaneously produces VAR and large current harmonics.

The per phase equivalent circuit is shown in Fig. 2 and the schematic control block diagram of the combined active power filter is shown in Fig. 3.

Since the main NPC converter is responsible to supply the fundamental VAR requirement of the load, its current is compared with the fundamental reactive load current. The error is processed through a PI controller to control the voltage delay angle $\delta$, so that the fundamental of the main converter current is indirectly controlled accordingly to the following equation.

$$I_{main} = \left( \frac{V_s - V_{cml} z - \delta}{Z_{main}} \right)$$

where, $V_s$ is the supply voltage, $V_{cml}$ is the fundamental voltage component of the main converter, $Z_{main}$ is the impedance of the inductor ($L_m$) connecting the main converter to the supply, and $I_{main}$ is the fundamental main converter current.
With the information of $\delta$, the modulating signals are adjusted to trigger the main converter switches. Hence the main converter current is indirectly controlled to meet the reactive current demand of the load.

To keep converter’s 5th and 7th harmonics low, the NPC converter firing angle has been chosen to be $\alpha = 15^\circ$ [3].

![Fig. 2 Per phase equivalent circuit and phase voltage of the main converter](image)

The per-phase equivalent circuit and the phase voltage waveform of the main converter are shown in Fig. 2.

![Fig. 3 Control block diagram shown for equivalent one phase](image)

**A) Estimation of Utility/ Source Reference Current**

It is desirable that the utility should supply the active component of load current and the loss component of the converters at unity power factor. Therefore, the supply current should be fully active (i.e., in phase with the respective phase voltage). In ideal case, the angle $\delta$ is supposed to be zero, as the main converter current should be only reactive in nature (as to cater the load reactive current) and in quadrature with the supply voltage. However, because of the converter losses, the capacitor voltage tends to fall and requires to draw some amount of active current from the supply to maintain the charge. So the angle $\delta$ acts as a measure of converter losses and a control signal proportional to $\delta$ is added with the active component of load current to determine the reference magnitude of the source current. This amplitude multiplied by a sin-template (in phase with corresponding utility phase voltage) gives the reference magnitude of the source current.

The difference between the actual supply current and the reference current acts as the reference for the auxiliary converter. The error is processed through a hysteresis controller to determine the switching of the converter. Here the dc link voltage is not compared with a pre-specified reference. It increases or decreases according to the VAR requirement of the load.

Inverter with low impedance and fast response tends to be overloaded in case of transient situation. So the auxiliary converter is not triggered initially. When the main converter current reaches a steady value and the VAR of the load is supplied locally from the main converter, the utility supplies the active component of current with some higher order harmonics. After the auxiliary converter is switched on, the higher order harmonic currents are supplied from the auxiliary converter and the utility supplies only the fundamental active component of current.

**IV. SIMULATION STUDY**

Detailed simulation studies are carried out with SABER simulator to observe the performance of the combined compensator with the proposed control law.

Initially, the main converter is switched on, and after the current has reached the steady state, auxiliary converter is triggered on. Some typical results are presented to validate the control scheme.

The effect of individual converters on utility current and their steady state performance is presented in Fig. 4.

Fig. 4 shows the supply voltage, supply current and load current of phase A. The load current is having displacement factor of 0.66 (lag). The load current r.m.s is 148 A. The total load is of the order of 100 kVA. The load current THD is 15.1%. Initially, the auxiliary converter is not switched on. The main converter supplies the fundamental reactive current to the load. But it cannot compensate for the current harmonics and the supply current THD is found to be 17.9% (first five cycles in Fig. 4) as
shown in Fig. 6. As the auxiliary converter is switched on, the supply current is bound within a hysteresis band, and then the utility current THD reduces to 4.4% (Fig. 7), and supply power factor becomes nearly unity (0.996).

At 100 kVA load, the ratio of auxiliary current to the main converter current is approximately 25%.

The load kVA has been increased from 100 to 120 kVA. Once the two converters lock the phase of the utility voltage and current to unity power factor condition, the dynamic change in load is also mitigated at the same condition without change in power factor. Momentarily the transient reactive current demand of the load is taken care by the fast acting auxiliary converter. But as soon as the main converter current builds up to meet the increased load VAR, the current of the auxiliary converter reduces. Corresponding increase in dc link voltage is observed in Fig. 5 indicating the dependence of VAR to be compensated on the dc link voltage.

V. CONCLUSION

A new parallel converter topology and control strategy has been investigated and reported in the present paper. For high power loads, which consume large VAR and harmonics, this combination of parallel filter has been shown to be useful, as the combination of high power low frequency devices and low power high frequency devices utilizes the devices to their full capacity. SABER simulation results verify the effectiveness of the proposed scheme with a nonlinear load having substantial amount of reactive and harmonic currents.

Fig. 4 The effect of auxiliary converter and steady state results

Fig. 6 Harmonic spectra of NPC – APF scheme for nonlinear load compensation

(a) supply current of Phase-A (without auxiliary converter), (b) Load current of phase-A

Fig. 5 Dynamic performance (Vdc has been shown in reduced scale Vdc/100)

Fig. 7 Harmonic spectra of supply current (phase-A) with auxiliary converter ON

REFERENCES