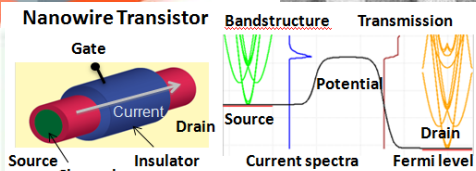
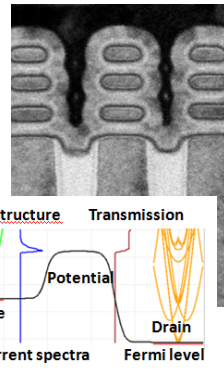
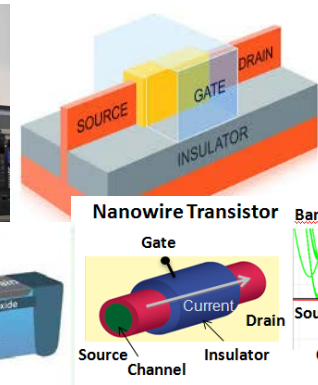


Modeling and Simulation of Nano-Transistors

JULY 6 - 10, 2020

Department of Electrical Engineering, IIT Kanpur



Website

<http://www.iitk.ac.in/nanolab/sc2020>

Registration Form

<http://www.iitk.ac.in/nanolab/sc2020>

Registration Fee *

Industry/R&D Labs: Rs. 25,000

Faculty: Rs. 5,000

Students: Rs. 5,000

*Registration Fee includes course fee, accommodation, meals, printed lecture notes and stationery.

Coordinator

Prof. Y. S. Chauhan, IIT Kanpur

Contact

nanolab.iitk@gmail.com

Topics:

- VLSI design and Nanoelectronics
- Physics and Operation of MOSFET
- SPICE and Circuit simulation
- TCAD simulation: Theory and demonstration
- Compact Modeling: Theory and demonstration
- Scaling and Moore's Law
- Nano-Transistors: FinFET, FDSOI, Negative Capacitance FET
- Nanosheet FETs, 2D-FETs etc.
- Characterization: Current and capacitance measurement
- RF CMOS and GaN High Electron Mobility Transistors

Also included:

- Laboratory visits and RF transistor measurement
- New research problems in Nanoelectronics
- How to write research project and papers

Target Audience:

Faculty members, practicing engineers & students.

Hands-on Sessions: Verilog-A coding, SPICE ckt. Simulation, TCAD Simulation, Parameter Extraction

SPEAKERS



B. Inguiz
URV Spain

Fellow IEEE



S. Mahapatra
Dept. of EE
IIT Bombay

Fellow IEEE



Mansun Chan
HKUST
Hong Kong

Fellow IEEE



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Dame

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