PLL APPLICATIONS

Contents

1 Introduction

The PLL is one of the most commonly used circuits in electrical engineering. This section discusses the most important PLL applications and gives guidelines for the design of these circuits. A detailed discussion of different applications is beyond the scope of this article; for a comprehensive survey see [1] and [2].

The baseband model of analog phase-locked loop and its linear theory were discussed on the lecture. In all PLL applications, the phase-locked condition must be achieved and maintained. In order to avoid distortion, many applications require operation in the linear region, that is, the total variance of the phase error process resulting from noise and modulation must be kept small enough. If the PLL operates in the linear region then the linearized baseband model may be used in circuit design and development.

Recall that only the PD output, VCO control voltage, input phase $\theta_i(t)$ and output phase $\theta_o(t)$ appear in the PLL baseband model. All these signals are low-frequency signals. The RF input and output signals may be expressed from $\theta_i(t)$ [see Eqs. (1) and (2)] and $\theta_o(t)$ [see Eqs. (8) and (9)], respectively.

Amplitude modulated (AM) signals may not be generated or processed by PLLs, even more, the PLL may be used to reject input AM.

In order to achieve the best circuit performance different phase detectors are used in the different applications, many of them are edge-triggered. A PLL may contain other edge-triggered circuits, a frequency divider, for example. The operation of PLLs including edge-triggered circuits may not be described exactly by the simple APLL model. However, Gardner has shown that the APLL theory may be used as a good approximation of the real operation if the closed-loop bandwidth is less than one tenth of the input frequency [3].

Sampling involved in edge-triggered operation and nonlinearity always increase the noise level. Consequently, if the input SNR is low than an analog multiplier has to be used as PD to get the best noise performance.

In addition to the conventional applications, new applications for the various PLLs have been published recently. It has been shown that both the analog [4] and sampling [5] PLLs may exhibit chaotic behavior.

Bernstein and Lieberman have proposed the application of an ideal sampling PLL for random number generation [6]. The quality of generated random numbers has been evaluated by the run test in [7].

2 Tracking Band-Pass Filter for Angle Modulated Signals

Because of their temperature dependence, narrowband bandpass filters cannot be implemented by conventional analog filters. In other applications, the carrier frequency of angle-modulated signal to be selected varies. These problems may be overcome if a PLL tracking the carrier is used as a bandpass filter. The PLL separates the spectrum of the angle-modulated signal from other interfering signals, or limits the transmitted spectrum to within specified bounds. The relationship between the input and output phase modulation is determined by the closed-loop transfer function

$$\Theta_o(s) = H(s)\Theta_i(s)\,. \tag{1}$$

Since differentiation in time corresponds to multiplication by s, the relationship between input and output FM is obtained from Eq. (1) as

$$s\Theta_o(s) = H(s)[s\Theta_i(s)]\,.$$

The filter characteristic is determined by the closed-loop transfer function. A further advantage of PLL bandpass tracking filter is that it rejects the amplitude modulation, that is, it may also be used as a limiter.

The block diagram of a bandpass tracking filter is shown in Fig. 1. If the loop parameters depend on the amplitude of the input signal, an AGC circuit must precede the PD in order to keep the filter parameters constant. Note that the problems of and the difficulties associated with the design and implementation of a high-frequency bandpass filter are reduced to the design and implementation of a baseband loop filter. The design of PLL bandpass filters is discussed in detail in [8].

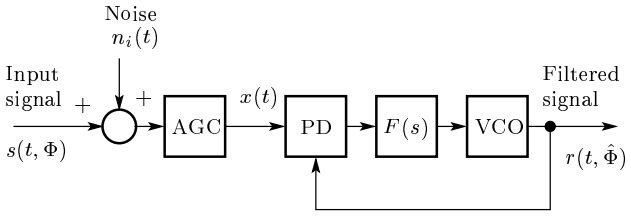

Figure 1: PLL configuration for band-pass tracking filter and CW carrier recovery. The AGC circuit is used to keep the input amplitude, that is, the loop parameters, constant.

3 CW Carrier Recovery

In every coherent receiver, the carrier has to be recovered from the noisy input signal [9]. Here, it is assumed that the carrier is present all the time in the received spectrum; the recovery of a suppressed carrier will be considered later. The aim of CW carrier recovery is to retrieve the carrier and to suppress as much noise, modulation, and interference as possible. The CW carrier recovery circuit is a narrowband bandpass tracking filter implemented by a PLL as shown in Fig. 1.

The noise-free recovery of a carrier in a noisy environment requires a very narrowband PLL. Unfortunately, the acquisition properties of narrowband PLLs are very poor. This problem may be eliminated by using two different loop bandwidths: a wide one during acquisition and a narrow one in steady-state, after the phase-locked condition has been achieved [10].

The Doppler effect must also be considered in many carrier recovery circuits. The ideal second-order PLL may track a frequency ramp, but the reduction of tracking error requires a wide loop bandwidth. Unfortunately, the noise-rejection performance of a PLL is inversely proportional to the loop bandwidth. For low SNR, this contradiction may be solved by using third- or higher-order loop configurations [11].

4 PLL Frequency Divider and Multiplier

The PLL may be used as a frequency divider if a frequency multiplier is placed into the feedback path as shown in Fig. 2, where M denotes the frequency-multiplier ratio.

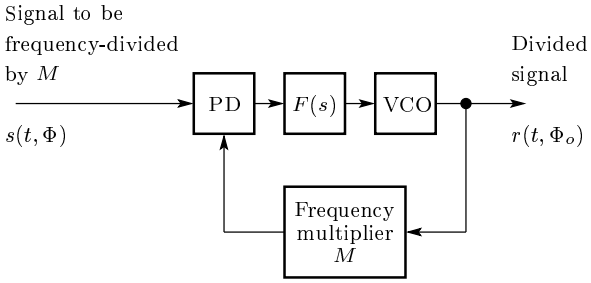

Figure 2: Block diagram of a PLL frequency divider.

Let ω_i denote the frequency of input signal $s(t, \Phi)$. Under phase locked condition the PLL divides the input frequency by M

$$r(t, \Phi_o) = \sqrt{2}V_o \cos \Phi_o = \sqrt{2}V_o \cos(\frac{\omega_i}{M}t + \theta_o).$$

When the carrier frequency of an angle modulated signal is divided, its modulation frequency f_m does not change, but its phase/frequency deviation is divided by M

$$\Theta_o(s) = \frac{1}{M}H(s)\Theta_i(s). \tag{2}$$

In Eq. (2) H(s) denotes the closed-loop PLL transfer function. However, the frequency multiplier in the feedback path increases the loop gain as shown by

$$K = MK_gK_dK_v.$$

The PLL may be used as a frequency multiplier if, instead of the multiplier, a frequency divider with division ratio of N is placed into the feedback path in Fig. 2. Again, the modulation frequency of angle modulated signal does not change, but the carrier frequency and the phase/frequency deviation is multiplied by N

$$\Theta_o(s) = NH(s)\Theta_i(s)$$

where the loop gain is

$$K = \frac{K_gK_dK_v}{N}.$$

5 PLL Amplifier for Angle Modulated Signals

The high-gain amplifiers operating in the extremely high-frequency bands are very expensive. The PLL may be used for amplification of angle-modulated signals, the signal to be amplified is applied to the PLL input and the VCO output is the amplified signal. The gain is determined by the ratio of VCO output and PLL input powers. Note that the amplification is performed in the baseband. In addition to amplification, the PLL also operates as a limiter and filter for the incoming angle-modulated signals.

Sometimes it is cheaper to implement the VCO and power amplifier below the input frequency band, as shown in Fig. 3. Due to the frequency multiplier placed in the feedback path, the VCO output frequency is f_i/M, where f_i is the input frequency. The input phase/frequency deviation is also divided by M; however, the modulating frequency remains unchanged. The output frequency multiplier following the power amplifier restores the original carrier frequency and its phase/frequency deviation.

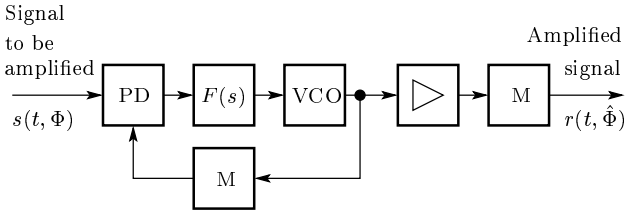

Figure 3: Amplification of angle-modulated high frequency signals by PLL.

6 Frequency Synthesis and Angle Modulation by PLL

Signals with high frequency stability and high spectral purity are often required in electrical engineering. In many applications, the frequency of generated signal must be varied by a digital code.

The PLL is widely used in frequency synthesis to generate spectrally pure signals and, if necessary, to operate as an analog or digital frequency or phase modulator. Frequency multiplication or division, frequency addition or subtraction may be performed, using a PLL in conjunction with programmable frequency dividers and mixers as shown in Fig. 4. As a result, the output frequency f_o depends on the reference f_R and offset f_S frequencies, moreover, on the division ratios of frequency dividers. In frequency synthesis, the PLL input is called *reference signal* and its frequency is denoted by f_R. To optimize the system performance, frequently a multiloop circuit configuration [12] is used.

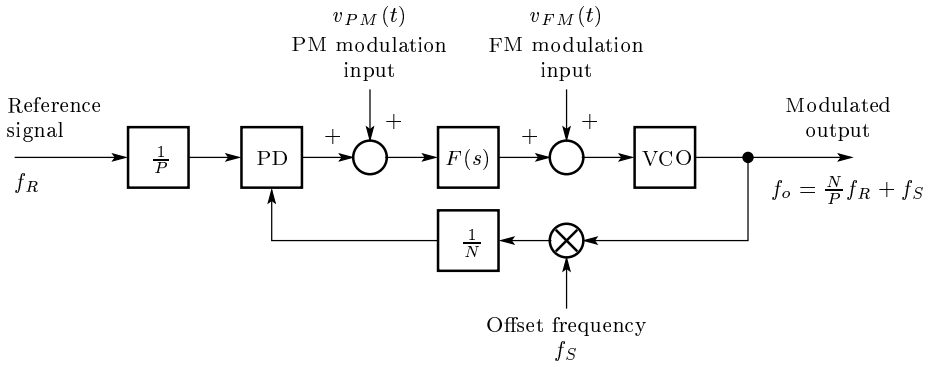

Figure 4: Frequency synthesis by phase lock.

In frequency synthesis, the dominant noise sources are the VCO, frequency dividers, mixers, and phase detectors. The main design goals are to minimize the output phase noise, to avoid the generation of spurious output signals, and to minimize the unwanted output FM caused by the periodic output of the phase detector. These requirements can be satisfied with special PD configurations, such as sample-and-hold phase detector or phase-frequency detector with a charge-pump circuit. The operation of these edge-triggered PDs and the analysis of PLLs implemented with them is discussed in the last section of the article.

Many system level aspects must be considered during the development of frequency synthesizers, a detailed discussion of these questions may be found in [12] – [15].

In addition to frequency synthesis, PLLs may be also used as FM or PM modulators. The corresponding transfer functions for FM and PM are

$$\begin{aligned} s\Theta_o(s) &= [1 - H(s)]K_v V_{FM}(s) \\ \Theta_o(s) &= H(s)\tfrac{N}{AK} V_{PM}(s) \end{aligned} \tag{3}$$

where K_v and $N/(AK)$ are the gains of the FM and PM modulators, respectively. $H(s)$ and $[1 - H(s)]$ denote the closed-loop transfer and error functions, respectively. However, since the frequency synthesizer has a frequency divider in the feedback path, the loop gain becomes

$$K = \frac{K_g K_d K_v}{N} \, . \tag{4}$$

7 Coherent Demodulation by APLL

The noise performance of coherent demodulators is much better than that of their noncoherent counterparts [9]. A circuit configuration which is suitable for coherent PM, FM, and AM demodulation is shown in Fig. 5.

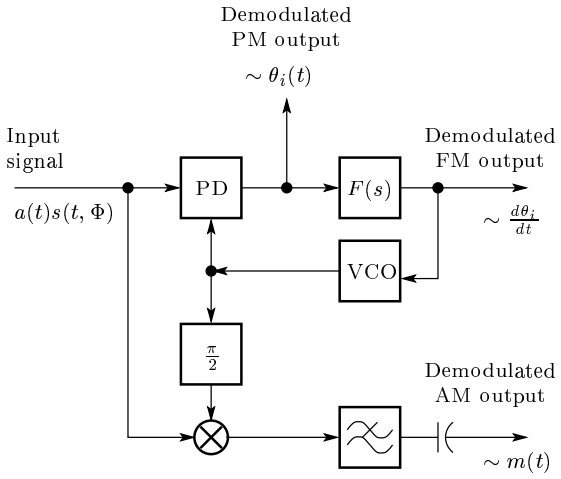

Figure 5: Coherent PM, FM and AM demodulation by APLL.

7.1 PM Demodulator

Assume first that the input signal $s(t, \Phi)$ is phase modulated and $a(t) = A =$ constant. The demodulated PM signal appears at the output of the phase detector

$$V_d(s) = [1 - H(s)]AK_d\Theta_i(s) \tag{5}$$

where $\Theta_i(s)$ denotes the input PM and AK_d is the gain of the PM demodulator. The demodulated PM signal is multiplied by the closed-loop error function which has a high-pass characteristic. Distortion is avoided if the closed-loop bandwidth is less than the lowest modulation frequency. The other source of distortion is the PD nonlinearity. This type of distortion does not appear if the total variance of the phase error given by remains small enough, that is, if the phase error remains in the close neighborhood of its steady-state value during the operation.

7.2 FM Demodulator

Assume that a frequency modulated input signal is applied to the PLL input. Due to the phase-locked condition, the VCO frequency follows the incoming frequency. Since the instantaneous VCO frequency is proportional to the VCO control voltage, the FM modulation may be recovered from the VCO control voltage. By means of the transfer function concept, the demodulated signal is obtained

$$V_c(s) = H(s)\frac{1}{K_v}s\Theta_i(s) \tag{6}$$

where $1/K_v$ is the gain of FM demodulator. This equation shows that the FM demodulator output, that is, the VCO control voltage, is proportional to the input FM if the closed-loop bandwidth exceeds the highest modulation frequency.

The distortion caused by the PD nonlinearity is reduced by feedback, consequently, the PD distortion is not critical. However, the VCO transfer function must be linear in order to get an FM demodulator with low distortion.

7.3 AM Demodulator

Let the input signal be amplitude modulated

$$x(t) = [1 + m(t)]\sqrt{2}A \sin(\omega_i t + \theta_{i0}) \tag{7}$$

where $m(t)$ carries the information, and A, ω_i and θ_{i0} are constants. The PLL demodulator contains a carrier recovery circuit (see the PLL in Fig. 5) and an AM demodulator (see the analog multiplier and low-pass filter in Fig. 5). Since the PLL needs an input signal to be tracked continuously, the spectrum of the AM signal must contain a carrier component.

The carrier is recovered by the PLL, its VCO output is

$$r(t, \hat{\Phi}) = \sqrt{2}V_o \cos(\omega_i t + \theta_{i0}). \tag{8}$$

This signal is multiplied by the AM input signal. The low-pass filter selects the difference-frequency output of multiplier and the DC blocking capacitor removes its DC component. The demodulated signal is obtained from Eqs. (7) and (8)

$$AV_o m(t) \tag{9}$$

where AV_o is the gain of the AM demodulator.

8 Suppressed Carrier Recovery Circuits

In digital telecommunications, the optimum detection of transmitted data requires that both the carrier and clock signals be available at the receiver [9]. The carrier and clock recovery circuits are used to retrieve these signals from the noisy digitally modulated received waveform.

In order to maximize the power efficiency, modern digital modulation techniques suppress the carrier completely, consequently, all transmitted energy resides in the data sidebands. Narrowband PLLs cannot be used for carrier recovery, because the carrier frequency is missing from the input spectrum.

The missing carrier can be regenerated by nonlinear circuits called *regenerators*. The regenerator may be placed before the narrowband PLL as an entirely separate circuit, or it may be included in the loop. Examples for the first and second solutions are the squaring and Costas loops, respectively.

Many factors have to be considered during the selection and development of a suppressed carrier recovery circuit [16]. Here, only the basic operating principles of these circuits are surveyed. For more details refer to [17, 10, 16], [18] – [20].

For the sake of simplicity, only *binary phase shift keying* (BPSK) modulation is considered here. In BPSK, the binary information to be transmitted is mapped to the phase of a sinusoidal carrier. If the data bit is a "1," the phase of the carrier is zero; while if the data bit is a "0," the carrier phase becomes $-180°$. If the probabilities of "1"s and "0"s are equal, then the carrier is completely suppressed. In the noise-free case, the received signal may be expressed in the form

$$v_i(t) = m(t) \sin(\omega_i t + \theta_i) \tag{10}$$

where ω_i is the carrier frequency and the carrier phase θ_i is arbitrary but constant. The binary data stream is given by $m(t) = \pm 1$. Three basic types of carrier recovery circuits are discussed here, the *squaring loop*, the *Costas loop* and the *inverse modulator*.

8.1 Squaring Loop

In this case, the nonlinear operation is performed by a square-law device, that is, a frequency doubler circuit. As shown in Fig. 6, the nonlinear operation precedes the narrowband APLL. From Eq. (10) the output of frequency doubler circuit is obtained

$$v_x(t) = v_i^2(t) = \frac{1}{2} m^2(t)[1 - \cos(2\omega_i t + 2\theta_i)]\,. \tag{11}$$

Since $m(t) = \pm 1$, $m^2(t) = 1$ and

$$v_x(t) \sim \cos(2\omega_i t + 2\theta_i)\,. \tag{12}$$

Equation (12) shows that, after the frequency doubler, a conventional narrowband PLL can be used to recover the second harmonic of the carrier. Finally, the double-frequency output of the PLL is frequency divided by two, in order to recover the original carrier.

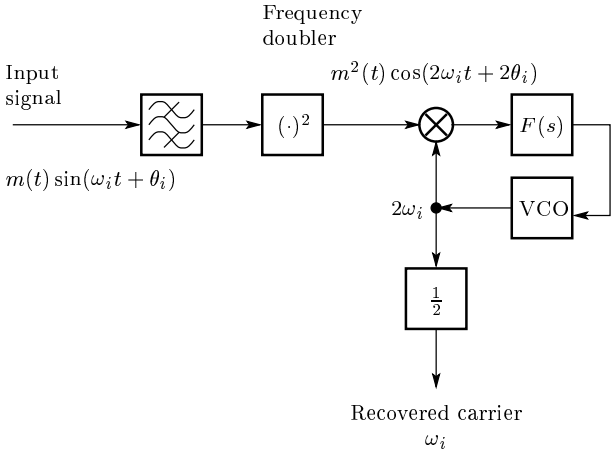

Figure 6: Suppressed carrier recovery by squaring loop.

8.2 Costas Loop

In the squaring loop the nonlinear operation is performed in the RF band. The Costas loop offers an alternative solution, where the BPSK modulation is removed in the baseband.

The block diagram of Costas loop is shown in Fig. 7. The circuit contains *in-phase* (I-arm) and *quadrature* (Q-arm) channels and an analog multiplier, that is, a phase detector which precedes the loop filter. The I- and Q-arms consist of an analog multiplier and a low-pass filter.

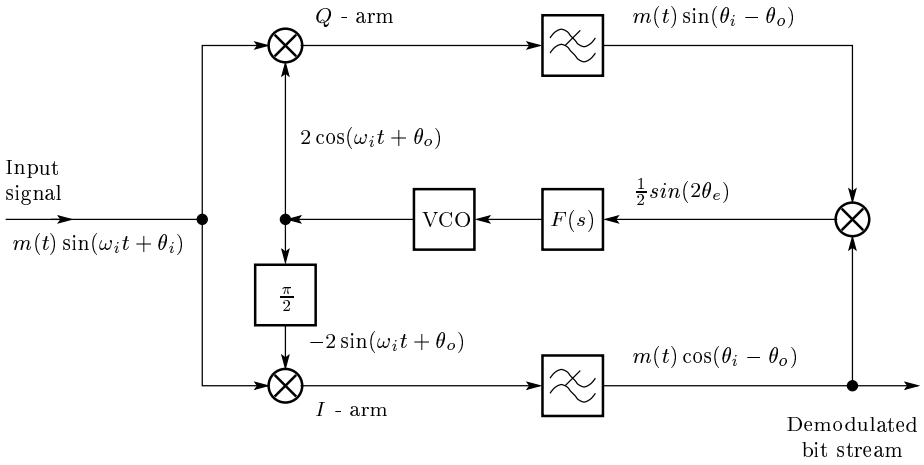

Figure 7: Demodulation of BPSK signal by Costas loop.

To understand the operation of Costas loop, assume that the phase-locked condition has been achieved and that the VCO output is

$$2\cos(\omega_i t + \theta_o)\,. \tag{13}$$

The output of low-pass filters in the Q- and I-arms are $m(t)\sin(\theta_i - \theta_o)$ and $m(t)\cos(\theta_i - \theta_o)$, respectively. Taking into account that $m^2(t) = 1$, the output of the baseband multiplier is obtained as

$$\frac{1}{2}m^2(t)\sin[2(\theta_i - \theta_o)] = \frac{1}{2}sin(2\theta_e)\,. \tag{14}$$

Equation (14) shows that, except a constant multiplier, the output of the baseband multiplier in the Costas loop is equal to the PD output of a conventional APLL in the noise free case. Consequently, the Costas loop behaves like an APLL.

In addition to carrier recovery, the Costas loop demodulates the incoming BPSK signal. If the phase error is small, then the output of the low-pass filter in the I-arm becomes

$$m(t)\cos(\theta_i - \theta_o) \approx m(t)\,. \tag{15}$$

8.3 Inverse Modulator

Two slightly different versions of inverse modulator or remodulator may be found in the literature [10]. The terms inverse modulator and remodulator are used interchangeably and indiscriminantly. As an example, the operation of an inverse modulator is discussed here.

The block diagram of an inverse modulator contains demodulator and modulator circuits, as shown in Fig. 8. Assume that the PLL involved has achieved the phase-locked condition and that the VCO output is

$$2\cos(\omega_i t + \theta_o)\,. \tag{16}$$

Then the output of the demodulator is obtained as

$$m(t - t_d)\cos(\theta_i - \theta_o) \tag{17}$$

where $(\theta_i - \theta_o)$ is the phase error of the PLL and t_d denotes the time delay of the low-pass filter involved in the demodulator. This demodulated signal modulates the recovered carrier in the modulator and produces an output

$$2m(t - t_d)\cos(\theta_i - \theta_o)\cos(\omega_i t + \theta_o) \tag{18}$$

which is multiplied in the phase detector by the delayed input signal $m(t-t_d)\sin(\omega_i t+\theta_i)$. The input signal has to be delayed in order to cancel the effect of delay in the demodulator.

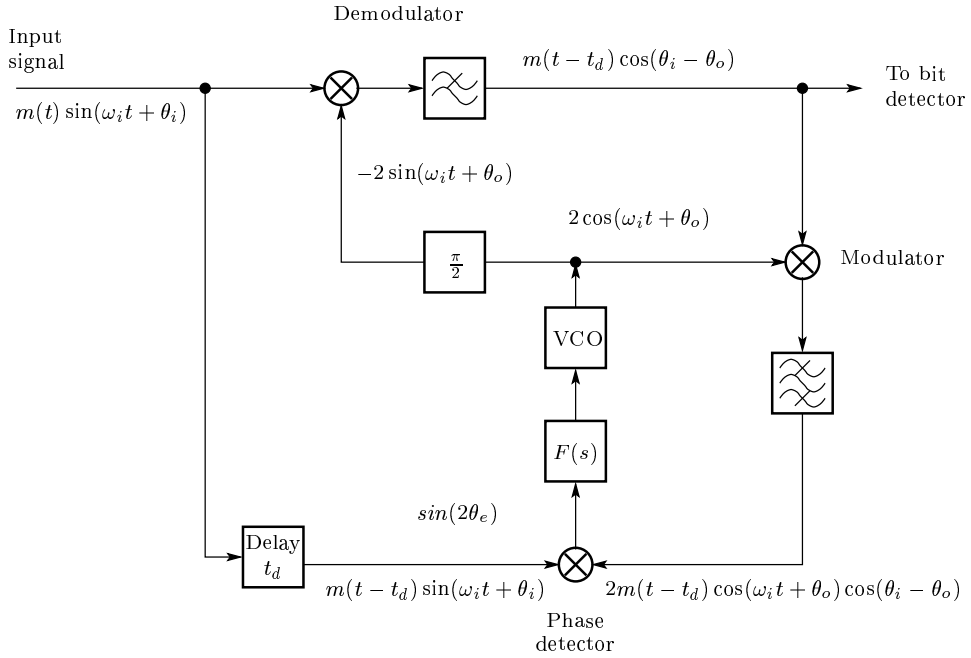

Figure 8: Block diagram of inverse modulator.

Neglecting the sum frequency component, the PD output is obtained

$$m^2(t - t_d)\cos(\theta_i - \theta_o)\sin(\theta_i - \theta_o) \approx \sin(2\theta_e)\,. \tag{19}$$

As in Eq. (14), this signal can be considered as the PD output of an equivalent PLL. Observe that if the phase error is small enough, then the demodulator output is equal to $m(t - t_d)$.

9 Clock Recovery Circuit

The timing information, that is, the clock signal, also has to be recovered in a digital telecommunication system [17, 16]. There are two basic classes of clock recovery circuits, but a PLL can be recognized behind both solutions.

The clock frequency component is regenerated from the incoming signal via some nonlinear operation in the first class of clock recovery circuits. These approaches offer the simplest solution, but their performance is only suboptimal. These solutions are analogous to the squaring loop used in suppressed carrier recovery. Examples for these circuits are the cross-symbol synchronizer [21] and the squaring loop symbol synchronizer [22].

The other class of clock recovery circuits is based on *maximum a posteriori estimation* (MAP) techniques [17, 23]. Many variants of this technique are currently used; they differ mainly in the phase detector (also called clock error detector) characteristics. The operation of the early-late gate clock recovery circuit [24], as an example, is discussed here.

The block diagram of the early-late gate clock recovery circuit is shown in Fig. 9. The circuit contains a pair of gated integrators called *early* and *late* gates, each performing its integration over a time interval of $T/2$. The input bit stream is

$$\sum_n a_n p(t - nT) \tag{20}$$

where T is the symbol duration and $p(t)$ denotes a rectangular pulse width duration T. Integration by the early and late gates are performed over the time intervals $T/2$, just before and after, respectively, the estimated location of data transition. Gate intervals adjoin each other, but do not overlap.

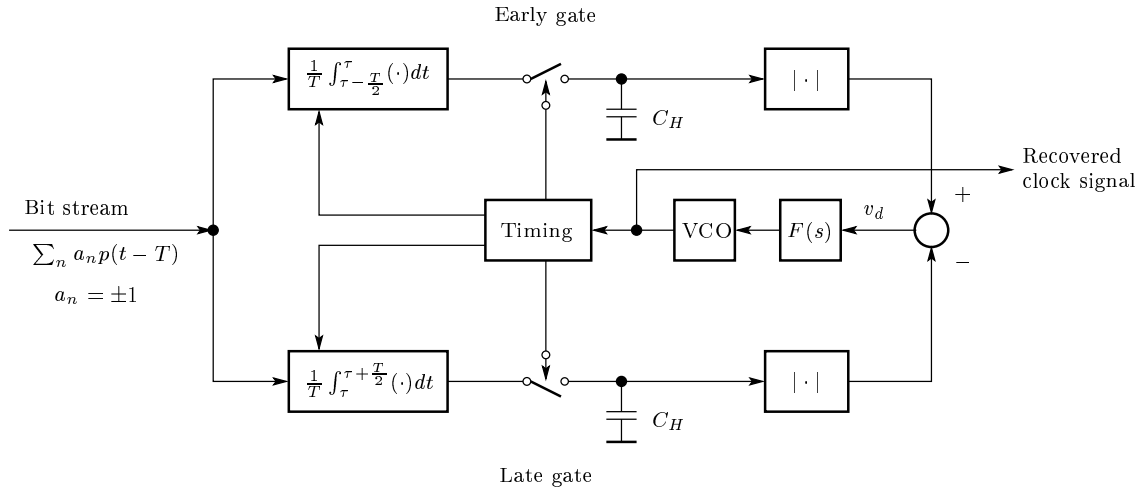

Figure 9: Block diagram of the early-late gate clock recovery circuit.

Waveforms helping to understand the operation of clock recovery circuit are shown in Fig. 10. If the timing error is zero, then the data transition falls just on the boundary between the operation of the early and late gates. In this case, the estimated and incoming data transitions coincide with each other, and the output of the two integrators, stored in the hold capacitors C_H, are equal. As a result, the error voltage $v_d(t)$ becomes zero.

Because the error voltage is produced from the absolute values of the integrator outputs, it is also zero if the data transition is missing.

If a transition of input data does not coincide with the estimated time instant of a transition, then a timing error denoted by τ in Fig. 10 appears. In this case, the data transition falls not on the boundary of operation of the early and late gates, but occurs within the operation interval of one of gates as shown in Fig. 10. Since the input signal changes its polarity during the gate operation, the associated integration reaches a smaller magnitude than for the other gate, where a transition does not occur. Comparing the magnitudes of the two integrators gives the error voltage $v_d(t)$ which is used after low-pass filtering to control the VCO frequency.

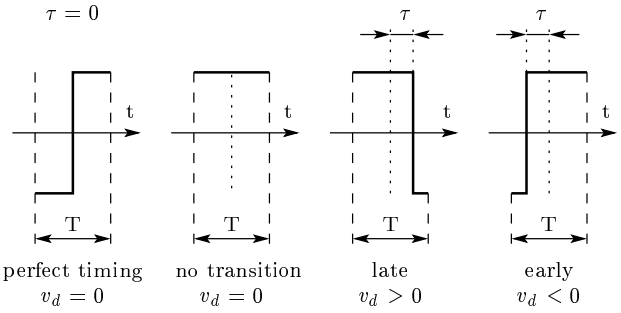

Figure 10: Typical waveforms in the early-late gate clock recovery circuit.

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