Current Copying Accuracy and Threshold Voltage Sensitivity in Current Driven Active Matrix Organic Light Emitting Display (AMOLED)

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Abstract: Current copying accuracy and stability of current through the organic light emitting diode (OLED) is of immense importance in current driven active matrix OLED display. This paper describes important parameters that impact copying accuracy through a systematic comparison of an idealized circuit consisting of ideal switches and a thin film transistor (TFT) based circuit. It is shown that the control voltage levels and parasitic capacitances have a significant impact on copying accuracy. Using the insight obtained through the analysis, the current mismatch between data and OLED current could be reduced below ±5% by proper choice of aspect ratio of the TFT for a range of 0-2μA. Impact of the threshold voltage shift of TFT on OLED current is also discussed.

Keywords: Organic light emitting display; active matrix; current driven pixel circuit;

Introduction Since the first observation of light emission in small molecule based light emitting diodes (OLEDS) [1], there has been increasing interest in their applications to large area flat panel displays (FPD) due to their adequate opto-electric properties, versatility of colors, large viewing angle and potentially low fabrication cost [2].

The OLED is a current driven device where the luminance is determined by the level of current flowing through it. This current can be provided by passive matrix (PMOLED) or Active matrix (AMOLED) architecture. In the later case, a thin film transistor (TFT) pixel circuit composes the matrix. This solution is preferred over the passive matrix approach, especially when the size of the display is increased. This is because passive matrix scheme requires high current level peaks through the pixel to obtain high luminance peaks [3]. This results in higher power consumption resulting in adverse effects on the OLED reliability. To modulate the OLED current in a active matrix display, current driving schemes with four TFT pixel electrode circuits have been proposed, whereby the current signal provided by external driver modulates directly the pixel electrode circuits [4]. Since the luminance of lighting element is proportional to its current density, therefore current-mode pixel driving approaches appear to be a natural solution for high quality OLED displays.

There are two key problems associated with current driven pixel circuits. The first one is mismatch between data and load current and the second is the sensitivity of load current to variations in TFT characteristics. This paper provides an understanding of key factors that affect these two outstanding problems and based on this understanding suggest a method of improving the copying accuracy.

Current driven pixel circuit and current mismatch: Several current driven pixel circuits have been proposed [4,5]. A popular 4-TFT (M_1, M_2, M_3, M_4), threshold voltage shift compensated current driven circuit is shown in Fig 1. Except for small changes, this circuit is equivalent to that presented in [4]. The input current during sample time is represented as I_{data} and the current through OLED during hold mode is represented by I_{load} .The transistors M_1, M_2 and M_3 act simply as switches while M_4 , the drive transistor, needs to act as an ideal current source.

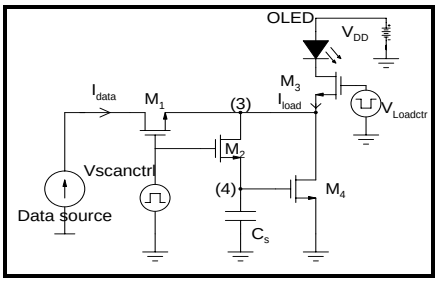

Figure 1: A 4TFT current driven pixel circuit

When the pixel is selected by forcing $V_{scanctrl}$ to high level of voltage, the transistors M_1 , M_2 are turned ON during the sample time and both the drain and gate voltage of M_4 are set by Idata., This voltage is variable and can differ from pixel to pixel and time to time, according to the desired current and magnitude of threshold voltage shift of M_4 of addressed pixel. Hence, the threshold voltage variation of M_4 is automatically adjusted by the current source on the data line. When M_1 and M_2 are switched off disconnecting the current source from the pixel circuit and M_3 is switched ON (hold mode), the circuit is expected to sink the same current as data current independent of process variations of circuit component for the rest of the frame period. However, several undesired factors, explained later, cause deviation in output current.

This deviation is quantified by defining current mismatch (CM) = $((I_{load}- I_{data}) \text{ X } 100/I_{data})$. Smaller the current mismatch, better is the copying accuracy of the circuit. It is well known that current in a TFT is a function of both gate to source voltage and drain to source voltage. The current in the hold mode would be same as that in sample mode if these two voltages of the

driver transistor M_4 does not change from sample to hold mode. A sample curve of gate to source voltage (V_4) and drain to source voltage (V_3) of drive transistor M_4 for a data current of 20μA while switching from sample to hold mode is shown in **Fig.2** for values of control signals and aspect ratios (W/L) as $V_{scanctrl}$=14V, $V_{loadctrl}$=10V, V_{DD}=18V, $(W/L)_1$=10μ/10μ, $(W/L)_2$= 10μ/10μ, $(W/L)_3$=25μ/10μ, $(W/L)_4$=40μ/10μ. The simulation was done using AIMSPICE simulator using *poly silicon TFT* model level-16. Spice model for OLED were taken from [6].The storage capacitor Cs is taken here as 5pF. Fig.2 shows a significant change in these two voltage which leads to current mismatch.

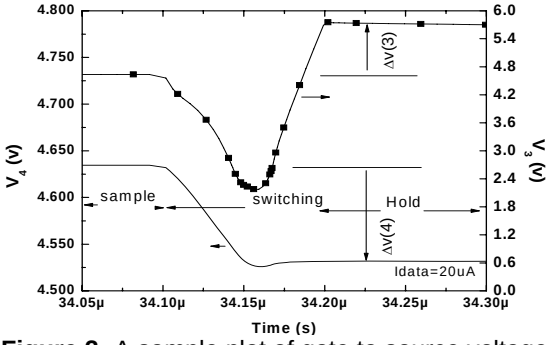

Figure 2: A sample plot of gate to source voltage V_4 and drain to source voltage V_3 of drive transistor M_4

In order to understand the causes of voltage change ΔV_4 and ΔV_3 as indicated in Fig. 2, an ideal circuit where transistors M_1, M_2 and M_3 are replaced by voltage controlled switches S_1, S_2 and S_3 and transistor M_4 is replaced by a voltage controlled current source was analyzed. The current source was chosen to be independent of the voltage V_3 and implemented as $I(vccs) = 1e^{-6} \times (V(4) - 2)2$. The control voltages for S_1 and S_2 are denoted as $V_{scanctrl}$ and for S3 it is denoted as $V_{loadctrl}$. The schematic is shown in Fig. 3. In this ideal pixel circuit, there are no parasitic capacitances and the voltage controlled current source has infinite output

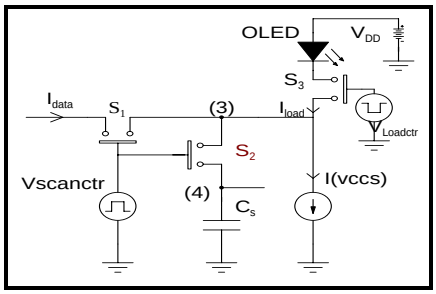

Figure 3: Schematic showing the replacement of transistors by Ideal switches and VCCS

resistance. The operation of this circuit is exactly same as the 4-TFT circuit. First of all, switches S_1 and S_2 are turned on and data current is passed during the programming time. When the switches S_1 and S_2 are turned off simultaneously to move into the hold mode, it is found that even in this ideal circuit, there is a drop in the storage capacitor Voltage (V_4).This occurs when switching is not instantaneous so that discharge path through S_2 exists momentarily. The change in storage capacitor voltage causes output current to change resulting in mismatch with respect to data current. The voltage V_4 across the storage capacitor can be maintained constant if S_2 is turned off prior to the S_1 so that the data current remains available during the time that S2 switches off. Fig 4**.** Shows the % change in current for the case where S_2 is turned off earlier and the case when S_1 and S_2 are switched simultaneously. For the former case, the capacitor voltage remains constant and mismatch

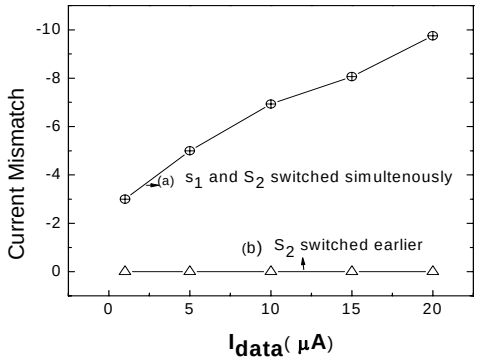

Figure 4: current mismatch Vs data current for two case (a) S_1 and S_2 switched simultaneously (b) S2 switched earlier than S1

between input and load current is zero. This is the perfect ideal condition where current mismatch is zero and **copying accuracy is 100%.** Since the thin film transistors has parasitic capacitances across its gate to source and gate to drain terminals, any sudden voltage change at one of the terminal will cause a change at the other terminal due to charge feed through. Hence different values of capacitances were placed in this ideal circuit between different nodes and individually their effect on current mismatch was observed. For example, placement of a capacitor between the controlling node of S_2 and node (4) will provide an approximate effect similar to that of the gate to source capacitance (C_{gs2}) of transistor M_2. Similarly, placement of a capacitor between node (3) and (4) will provide an approximate effect similar to that of gate drain capacitance (C_{gd4}) of drive transistor. Fig.5 and Fig. 6 show the effect on current mismatch of these two capacitances. The values of control voltages taken here are 10V and supply voltage was taken as 12V. Higher value of capacitances leads to a larger current mismatch in both the cases although the effects are of opposite nature. The negative effect on current due to C_{gs2} is basically because of the sudden change in $V_{scanctrl}$ (10 to 0V) which leads to a drop in V_4 and therefore decrease in current. To minimize the effect of C_{gs2}, the transistor M_2 should be kept at minimum size. The positive (negative) change in V_3 while moving from sample to hold mode is coupled to V_4 through C_{gd4} . This increases (decreases) V_4 and therefore the current. Change in V_3

depends on the supply voltage, drop across the OLED and drop across the switch and is higher for lower values of current. For the chosen supply voltage of 12volt, it was positive for the whole data range.

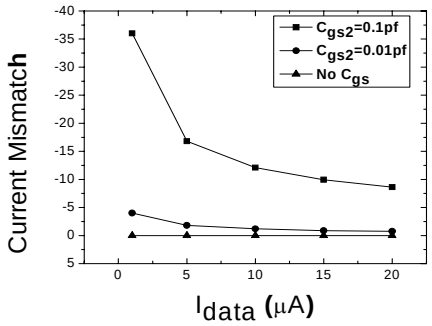

Figure 5: Impact of a parasitic capacitance (Cgs2) placed in Ideal circuit on current mismatch

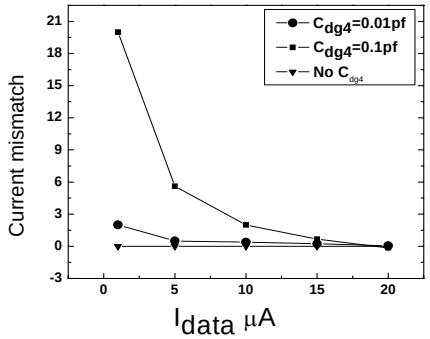

Figure 6: Impact of a parasitic capacitance (Cdg4) placed in Ideal circuit

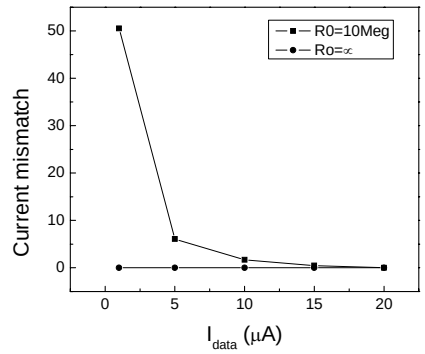

Figure-7: Impact of output resistance (R_o) of VCCS in Ideal circuit on current mismatch

It was observed through simulation that the parasitic capacitances associated with the other thin film transistors have negligible effect on the current mismatch. The impact of finite output resistance R_O of TFT M_4 on current mismatch can also be significant. To model this, a resistance Ro was added between the node (3) and ground in ideal circuit but all parasitic capacitances were removed so that effect of output resistance can be unambiguously studied. Fig **7** shows the impact on current mismatch as the out put resistance was varied from infinity to 10 Meg . As expected, a smaller output resistance coupled with larger change in V_3 leads to higher current mismatch at lower data current. The impact of output resistance is expected to be more important in Polysilicon transistors where Kink effect causes significant variation in current in saturation.

Current mismatch reduction by proper choice of aspect ratio (W/L): For the design, a data current (I_{data}) range of 0 to 2μA is assumed corresponding to a 2-4" display of QVGA resolution, maximum brightness of 500 Cd/m^2, aperture ratio of 50% and an OLED of efficiency 10Cd/A [6]. The value of storage capacitor (C_s) was kept fixed at 0.5 pf. The pixel sample time is 70μS for QVGA resolution and a frame rate of 60. The initial values of control voltage were taken as $V_{scanctr\ l}$= 8volt, $V_{loadctrl}$ = 8volt for the transistor sizes of 10μ/10μ. These voltage are selected such that the pixel gets properly programmed within the pixel sample time and the drive transistor operates in the saturation region for chosen data current range. Using minimum size transistors and control voltages as described above ***current mismatch*** of the circuit is shown in Fig.8-(b). A very large current mismatch of -49% occurs

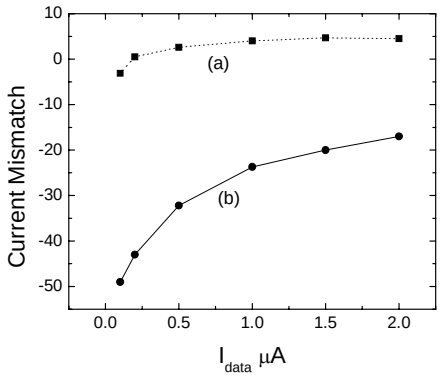

Figure 8: Two case of current mismatch (a) $(W/L)_1$ = 50μ/10μ, $(W/L)_2$=10μ/10μ, $(W/L)_3$ = 20μ/10μ, $(W/L)_4$=40μ/10μ, (b) All transistors of 10μ/10μ

at small currents. The large change in gate to source voltage V_4 of drive transistor M_4 is the main reason for the observed large current mismatch**.** Reduction in control voltage ($V_{scanctrl}$) by increasing transistor sizes could be a method to reduce the change in gate to source voltage. Increase in W/L of drive transistor (M_4) and transistor M_1 allows one to reduce the control voltage. Hence, the size of transistor M_1 was increased to 50μ/10μ and the size of the transistor M_4 to 40μ/10μ and $V_{scanctrl}$ was reduced to 6.5. Change in drain to source voltage can also be adjusted by changing the size of the transistor M_3 which was also increased to 20μ/10μ . By these changes, the current mismatch was found to be within ±5% for whole data current range and is shown in Fig 8-(a)

Threshold voltage shift and current mismatch: As explained earlier, the current mismatch occurs because of the changes in gate to source voltage (ΔV_4)

and change in drain to source voltage(ΔV_3) of drive transistor. A change in the threshold voltage of any transistor that affects these two voltages would lead to circuit becoming sensitive to threshold voltage. In order to quantify the impact of change in threshold voltage, the transistors were subjected to a positive threshold voltage shift of 1volt one by one and the impact on current mismatch was observed. Figures 9-11 show the impact of threshold voltages shifts on the current mismatch. The positive threshold voltage shift of transistor M_2 resulted in the positive shift in the current mismatch while it is negative for M_3 and M_4.

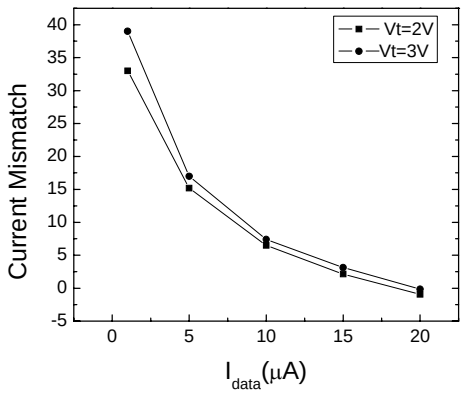

Figure 9: Impact of threshold voltage shift of M_2

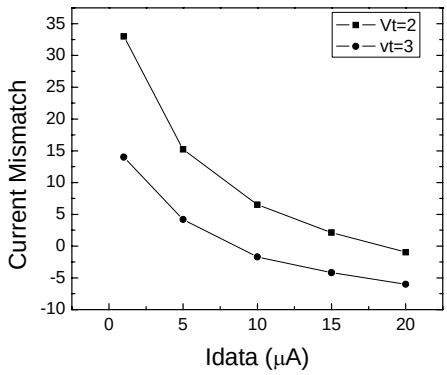

Figure 10: Impact of threshold voltage shift of M_3

The sensitivity to threshold voltage variation (S_{vt}) defined as the ratio of percentage change in load current to the percentage change in the threshold voltage is shown in Fig. 12. Two curves are shown corresponding to different values of VKINK voltage in TFT model. It can be clearly seen that the presence of significant kink in the output characteristics of the poly silicon transistor (meaning a small VKINK voltage) significantly increases the threshold voltage sensitivity. The reason is that a change in drain-source due to change in threshold voltage causes more change in the OLED current due to reduced output resistance.

Summary: In summary, an analysis of impact of control waveform voltages and TFT sizes on current copying accuracy has been described. It is shown that although a small value of control voltage results in reduced clock feedthrough effects, this voltage cannot be arbitrarily reduced as it increases TFT resistance causing incomplete charging of storage capacitor. The problem can be overcome by increasing TFT sizes but this also leads to increased parasitic capacitances. Based on an understanding of these effects, the TFT circuit was optimized to obtain accuracy better than 5%.

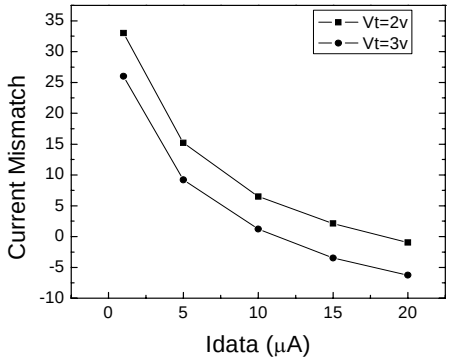

Figure 11: Impact of threshold voltage shift of M_4

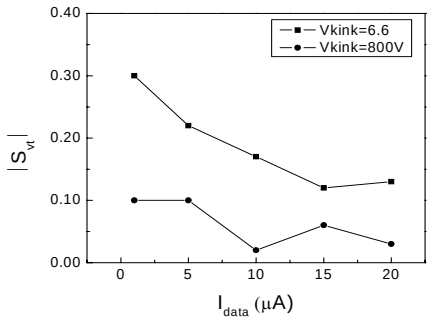

Figure 12: Threshold Voltage Sensitivity (S_{vt}) in poly-silicon TFT for two value of Vkink voltage

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