

A Low Power Wide Range CMOS Poly-Si Level Shifter for Active Matrix Display

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Abstract: We have designed and fabricated a wide range CMOS poly-Si level shifter. The proposed circuit employs 4 capacitors and 2 clocks (0~3V) to generate level-up signal (3~6V) and level-down signal (-3~0V). The generated level-up signal and the level-down signal make an amplified signal of full range (-3~6V). The power consumption of the level shifter was verified to be very low by SPICE simulation. The operation of fabricated level shifter was proved successfully at the high frequency of 1MHz.

Keywords: poly-Si TFTs; level shifter; CMOS

Introduction

Recently, the intergration of the pixel elements and peripheral driver has attracted a considerable attention for reducing the external driving circuitry and fabrication costs [1-5]. Low-temperature poly-Si (LTPS) TFTs are widely used for a pixel elements in the active-matrix liquid crystal display (AMLCD) and the active matrix organic light emitting diode (AMOLED) due to its high mobility and large on-current [1]. In the poly-Si TFT technology, the system-on-glass (SOG) display attracted a considerable attention [2-3]. CMOS poly-Si TFTs are widely used for circuit integration because the typical CMOS design scheme may be provided.

PMOS integration, which uses only p-type poly-Si TFTs for the pixel and driver panel, has been developed for panel integration to implement the SOG technology [4-9] because of its merits such as driving reliability and the fabrication-cost benefits compared with CMOS process. Despite LTPS p-type process provides reliability and cost benefits, the performance of integrated driver and the power consumptions can be worse than those of CMOS process [4]. It is rather difficult to design digital building blocks as well as analog circuit using p-type design compared with well-known CMOS design.

To achieve the peripheral circuits with low power consumption which are essential to mobile displays, especially, low voltage inputs and little current flows are required. The level shifter which has the capability of generating a wide range output signals, can be useful to operate integrated shift register and to switch pixel circuits.

The purpose of our work is to propose a new CMOS poly-Si level shifter which exhibits low power consumption and a wide range output for active matrix displays. The proposed circuit was verified by a simulation and the fabricated circuit was measured.

Conventional Level-Shifter

The conventional level-shifter composed of an amplifier and buffer is shown in Fig. 1. In the amplifier part, the level shifted signal (0~6V) is generated by the control of input signals (0~3V). During the operation, the penetrating current exists from VDD to VSS in the amplifier part. The power consumption of the level-shifter can be increased according to the dissipated currents. The conventional level-shifter is disadvantageous for fabricating integrated circuits with low power consumption.

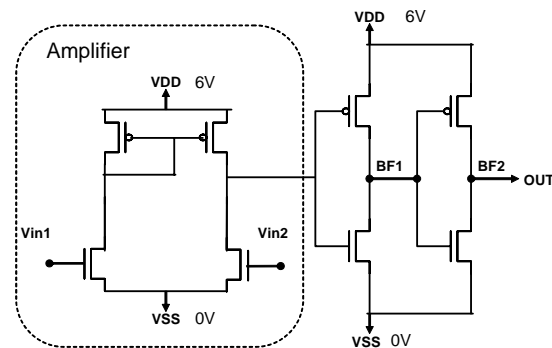


Figure 1. Conventional CMOS level-shifter

Proposed Level-Shifter

The proposed level shifter is composed of level shifting part and buffer as shown in Fig. 2. The amplifier part consists of 3 p-type poly-Si TFTs, 3 n-type poly-Si TFTs, 4 capacitors. And the buffer is composed of a chain of 2 inverters. 1 phase clocks (CK/CKB) with 0~3V swing and 4 DC inputs (0V, 3V, -3V, 6V) are needed to generate wide range output (-3V~6V). A high range signal (3~6V) is generated at the node "A" by a 2 n-type TFTs, 2 capacitors and input clocks. The operational schematic of the level-up component is shown in Fig. 3. When CLKB is high (3V), the gate voltage of N2 is increased by capacitor (C1) coupling. Then, N2 is turned on and node "A" is set to 3V. When CLK becomes high and CLKB becomes low, the voltage of node "A" rises to

6V by capacitor (C2) coupling and the N1 is turned on. The gate of N2 is kept to 3V and remains as off state to hold the voltage of node "A" to be 6V. Eventually, the level-up shifted signal (3~6V) is generated by iterative transition of input signals, CLK and CLKb. As the transition of input signals are repeated, the output signal at node "A" becomes stable to be close to 6V and 3V.

Similar to the operation of level-up shifter, the level-down shifter is designed to operate employing capacitor coupling as shown in Fig.4. At the node "B", a low range signal (-3~0V) is also generated by a 2 p-type TFTs, 2 capacitors and input clocks, simultaneously. When CLKb is high and CLK is low, node "B" is maintained as -3V due to the capacitor (C4) coupling. And the voltage of node "B" rises to 0V, when the CLKb becomes low and CLK becomes high. Finally, the output signal with down-shifted level is generated at node "B".

Eventually, output signal with a wide range (-3~6V) can be generated at the node "C" using the level-up shifted output at node A and the level-down at node B as shown in Fig. 2. When voltage of "A" is 3V and "B" is -3V, the p-type TFT connected to the "C" is turned on and the n-type TFT is turned off, so that the "C" can be set to 6V. On the contrary, when the "A" and "B" are 6V and 0V, respectively, the node "C" becomes -3V. The final signal with wide range (-3~6V) is generated after the signal at "C" operate a buffer which is composed of 2 stage

inverter chain. During the level-shifting operation, there are no paths where static current can flow from VDD to VSS because all TFTs are connected to the coupling capacitors. And the dynamic current dissipation is only related with the charging and discharging of capacitors. However, the current caused by charge and discharge of capacitor can be little because the potential differences between electrodes of capacitors are supposed to be not altered.

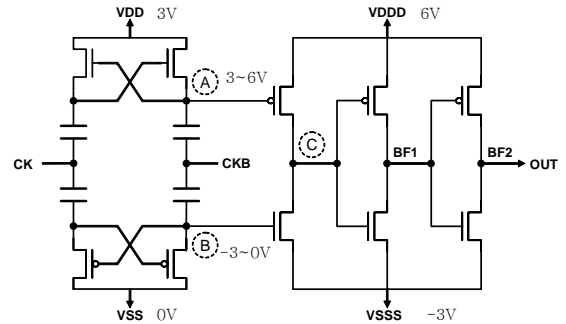


Figure 2. Proposed CMOS wide-range level-shifter by employing level-up and level-down voltage shifters

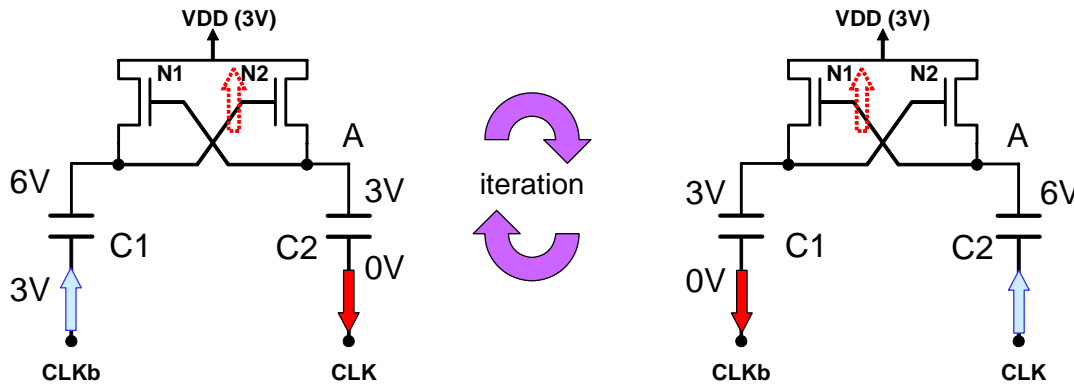


Figure 3. The schematic of operation of part for generating level-up signal (node A, 3~6V)

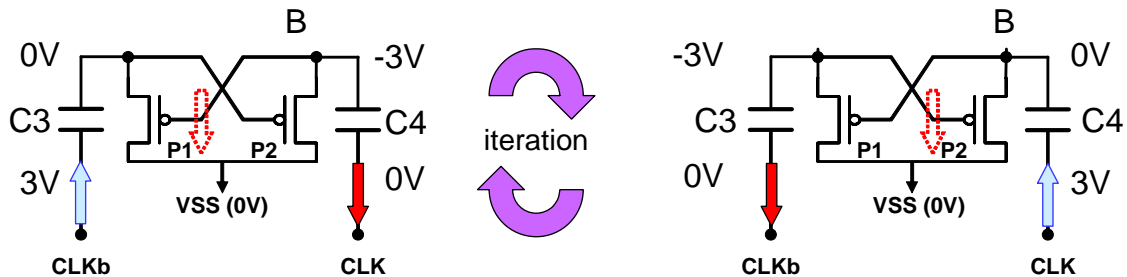


Figure 4. The schematic of operation of part for generating level-down signal (node B, -3~0V)

Fig. 5 demonstrates the input signals which is used to simulation of the proposed level-shifter. SmartSPICE program was employed for a simulation. When the input signals, CLK and CLKB, which have a swing of 3V, a frequency of 25KHz and opposite phase were applied to the input nodes, the level-up signal (3~5.7V) at node “A” and the level-down signal (-2.8~0V) are generated successfully as shown in Fig. 5. The level-up shifted signal of node “B” and the level-down shifted signal of node “A” are not identical to the expected voltage at each node (6V and -3V). The difference between simulation result and the expected voltage can be attributed to the little discharge of coupling capacitor when input signals have transient period such as a rising period and a falling period. During the transition of CLK, the TFTs which are connected to the VDD or VSS (N2 and P2) may not be turned off promptly, so that the swing of CLK can not be referred to the node “A” and node “B” perfectly.

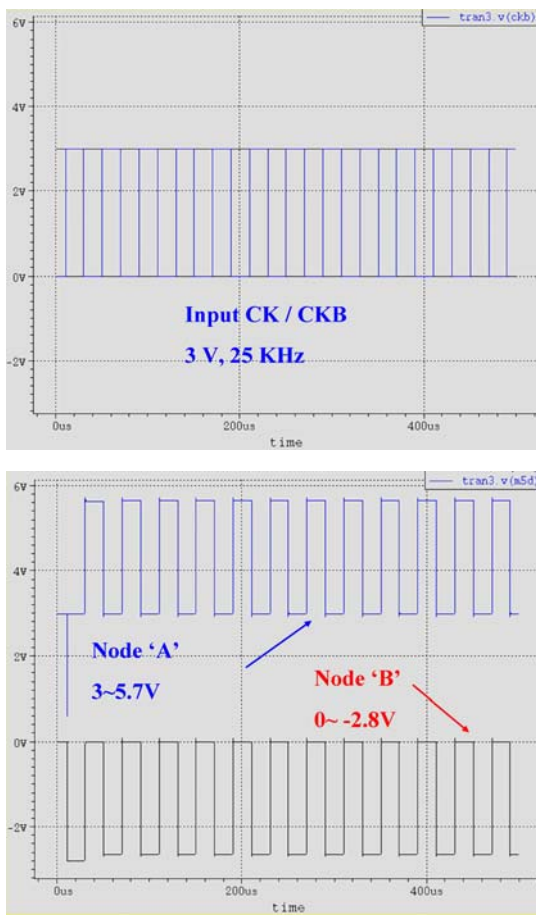


Figure 5. The input clock signals (upper) and the simulated result of node ‘A’ and node ‘B’ in the proposed level-shifter (lower)

The level-shifted signal with wide range from -3V to 6V generated at node “C” is verified by simulation as shown in Fig. 6. We can observe the proposed level-shifter can generate wide range level-shifted signal successfully. The currents dissipated at all nodes are demonstrated in Fig. 6. It is clear that there are no static currents during the

operation of the proposed level-shifter. When the input signals change from low to high or from high to low, dynamic currents are observed at some nodes. However, the duration time of currents dissipation is very short so that the power consumption of the proposed circuits can be reduced to a very low level compared with conventional ones.

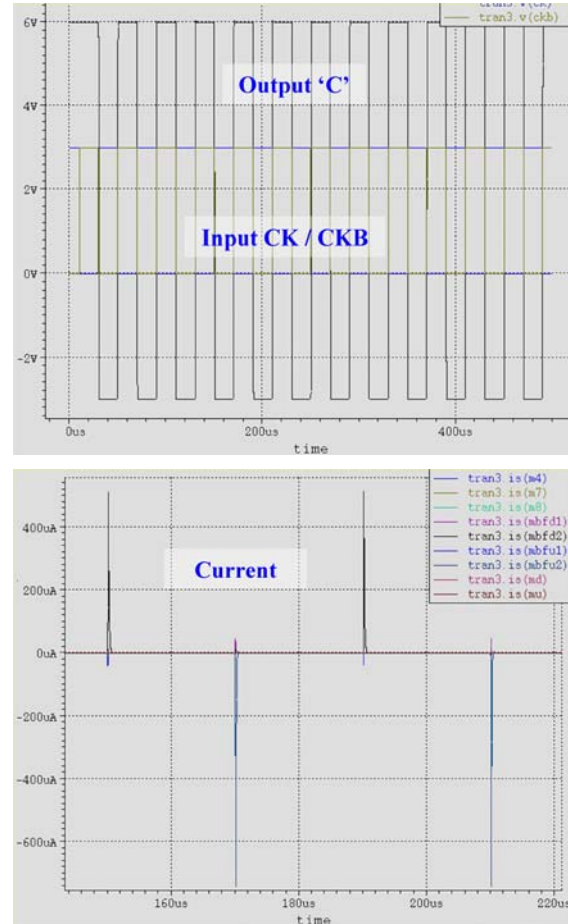


Figure 6. The simulated voltage of node ‘C’ in the proposed level-shifter (upper) and the currents generated at all nodes during the simulation (lower)

We have fabricated the proposed level-shifter on the glass employing conventional LTPS process. Fig. 7 shows the measured result of the proposed level-shifter of which operation frequency is 50KHz. The measurement was performed using Tektronix TDS784D. A full range (-3~6V) output was generated by input clock signals of which swing is 0~3V. A little rising and falling delay can be found at the measurement graph. The delay can be attributed the output load which is composed of the output load capacitor (10pF) which is connected to the metal pad for measurement and the external impedance of measuring probes.

The fabricated level-shifter was operated successfully at the high speed of 1MHz as shown in Fig. 8. The proposed level-shifter is proved to generate output signal

with wide range (-3~6V) at same time without any additional level-down circuit.

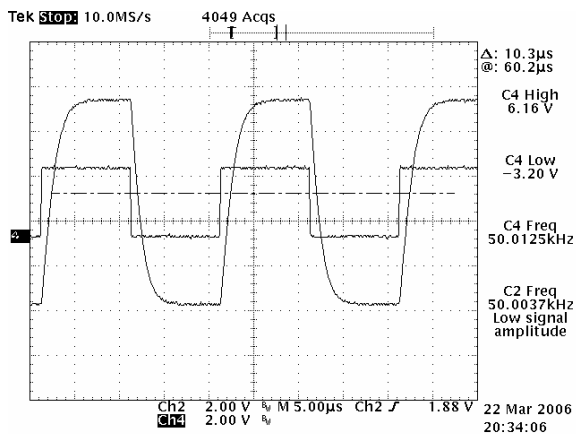


Figure 7. Measurement results of the proposed level shifter (input frequency = 50KHz)

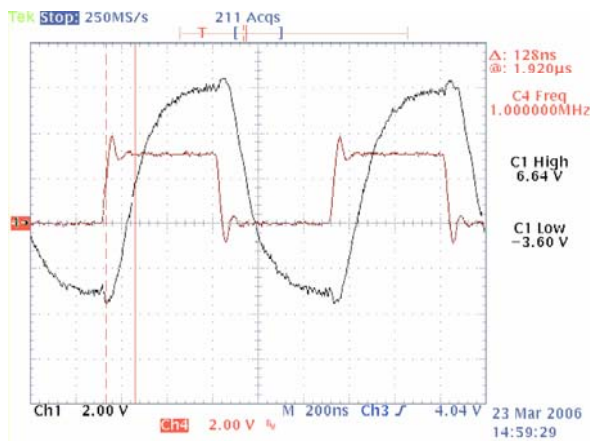


Figure 8. Measurement results of the proposed level shifter (input frequency = 1MHz)

Conclusion

We have designed and fabricated a wide range CMOS poly-Si level shifter. The proposed circuit employs 4capacitors, 2 n-type TFTs, 2 p-type TFTs and 2clocks (0~3V) to generate level-up signal (3~6V) and level-down signal (-3~0V). The generated level-up signal and the level-down signal make an amplified signal of full

range (-3~6V). The power consumption of the level shifter was verified to be very low by SPICE simulation. The operation of fabricated level shifter was proved successfully at the high frequency of 1MHz. The simulation and measurement results ensure that the proposed circuits are successfully designed for CMOS panel integration with low power consumption.

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