Shared Pixel Compensation Circuit for AM-OLED Displays

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Abstract: *We propose a novel cathode-common compensation circuit with a shared pixel compensation circuit technology for an nMIS TFT backplane that is used for a-Si AM-OLED displays. We can reduce the number of TFTs and capacitors per pixel to two TFTs and one-half capacitor by applying this technology to a 2 ×2 RGBW AM-OLED pixel configuration.*

Keywords: Active matrix; organic light-emitting diode; pixel circuit; compensation circuit; thin-film transistor; shared pixel circuit.

Introduction

Organic light-emitting diode (OLED) displays are presently of compelling interest because of their advantages to other displays, such as high brightness, high contrast ratio, fast response time, wide viewing angle, wide gamut, low power consumption, etc.

In the case of active-matrix OLED (AM-OLED) displays, the nonuniformity of gray levels is a severe problem that is caused by the nonuniformity of the mobility and the threshold voltage (V_T) of the driver thin-film transistors (TFTs); therefore, many compensation circuits and driving techniques were proposed. However, those proposed pixel circuits usually required more than three TFTs and a number of capacitors per pixel. In addition, it was very difficult to preserve enough of the emission area to accommodate the bottom-emitting OLED structure, and such a high number of electrical parts diminished the production yield of the displays.

Kwak *et al.* proposed a novel driving method called "TDC: Time Division Control", and they pointed out that

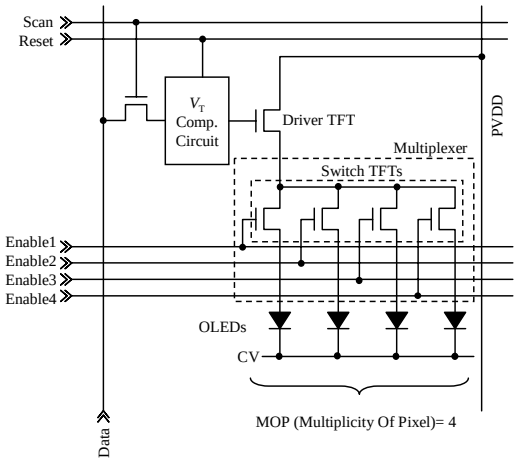

Figure 1. Concept of shared pixel circuit for an nMIS TFT circuit

the sharing technique reduces the number of required TFTs per pixel by showing the example of the pMIS TFT pixel circuit [1].

On the other hand, if we target large-sized AM-OLED displays, amorphous silicon (a-Si) TFT technology is a likely candidate. In addition, if we can decrease the number of TFTs by using sharing technology, it will contribute to the improvement of the production yield. However, it is difficult to apply the conventional pixel circuits to a sharing technology because the nMIS transistor circuits are only available for a-Si technology. For example, the proposed circuit by Jung *et al.* [2] is not suitable for sharing technology because we have to introduce three transistors that are connected to the OLED in series, if we simply apply their circuit to the technology.

In this paper, we propose a novel pixel compensation circuit for solving this difficulty, and we show a driving scheme. We also present an example of the pixel layout for a bottom-emitting a-Si AM-OLED displays.

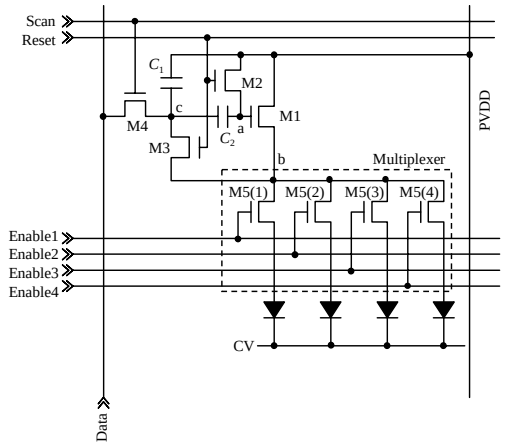

Figure 2. Proposed pixel circuit (MOP = 4)

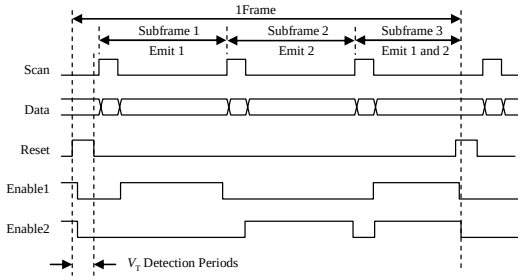

Figure 3. Example of the timing chart for proposed circuit in case of MOP = 2

Concept of the Shared Pixel Circuit for an nMIS TFT Circuit

Figure 1 shows the concept of the shared pixel compensation circuit. Two nMIS TFTs are connected to each OLED in series. Here, we call the number of multiplexed OLED devices the multiplicity of pixels (MOP); for instance, Fig. 1 is the case of MOP = 4, and each OLED is red, green, blue, or white. The multiplexing transistors work not only as a multiplexer but also as a switch of the pixel to detect the V_T of driver TFT.

Principle of the V_T Compensation Circuit

We propose the novel V_T compensation circuit, as shown in Fig. 2, which is based on the concept in Fig. 1. The compensation unit consists of two TFTs and two capacitors, i.e., three TFTs and one capacitor per subpixel for MOP = 2, and two TFTs and one-half capacitors per subpixel for MOP = 4. Figure 3 shows the timing chart for the pixel circuit in Fig. 2 for MOP = 2.

The "V_T detection periods" are established at the end of each frame or subframe by changing the potential of the "Reset" line from a low level to a high level. Then, node *c* is connected to the source electrode of driver TFT (node *b*), and node *a* is connected to the drain electrode of the driver TFT. Here, all of the "Enable" lines are at a low level, therefore the driver TFT is isolated from any OLED devices, i.e., the equivalent circuit at this period is as indicated in Fig. 4. At the end of the period, the potentials of each node are:

$$\begin{aligned} V_a &= V_{DD} \\ V_b &= V_{DD} - V_T \\ V_c &= V_{DD} - V_T \end{aligned} \quad . \qquad (1)$$

Next, the Reset line is changed to a low level, and the "Scan" line is changed to a high level. The data signal, V_{data}, is programmed into the pixel. Then,

$$\begin{aligned} V_a &= V_{data} + V_T \\ V_b &= unknown \\ V_c &= V_{data} \end{aligned} \quad . \qquad (2)$$

Therefore, the potential difference between nodes *a* and *c* is always kept at V_T by C2. Here, if the potential fluctuation by the charge leakage from node *a* to

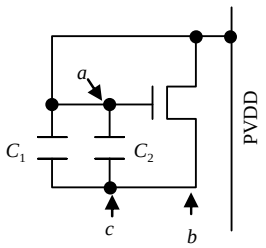

Figure 4. Equivalent circuit at V_T detection periods

Table 1. Pixel parameters for SPICE simulation. Mn (n = 1 to 5) indicates the size of the transistors (*W*/*L*)

M1	245 μm/4 μm	**M5**	112.5 μm/4 μm
M2	20 μm/4 μm	**C1**	0.44 pF
M3	20 μm/4 μm	**C2**	0.44 pF
M4	60.5 μm/4 μm	**MOP**	2

anywhere is smaller than the data voltage level for the gray scale of the least significant bit (LSB), then one V_T detection period per a frame is enough.

After writing the data, any "Enable" line is changed from a low level to a high level. Then, the potentials at each node are:

$$\begin{aligned} V_a &= V_{data} + V_T \\ V_b &= V_{OLED} \\ V_c &= V_{data} \end{aligned} \quad , \qquad (3)$$

namely, the pixel current for driver TFT is:

$$\begin{aligned} i_{pixel} &= \frac{\beta}{2}\left(V_{gs} - V_T\right)^2 \\ &= \frac{\beta}{2}\left(V_a - V_b - V_T\right)^2 \\ &= \frac{\beta}{2}\left(V_{data} + V_T - V_{OLED} - V_T\right)^2 \\ &= \frac{\beta}{2}\left(V_{data} - V_{OLED}\right)^2 \end{aligned} \quad , \qquad (4)$$

where, β is:

$$\beta = \frac{W}{L}\mu_{FE}C_{ox} \quad , \qquad (5)$$

and *W*, *L*, μ_{FE}, and C_{ox} are the channel width, the channel length, the field-effect mobility of the driver TFT, and the gate oxide capacitance of the driver TFT, respectively.

This indicates that the pixel current is theoretically independent of the threshold voltage, and the OLED emits light in accordance with the pixel current.

Simulation

To verify the functionality of the pixel circuit, we simulated the circuit with the pixel parameters listed in Table 1 and an amorphous silicon TFT model created by Rensselaer Polytechnic Institute [3].

As shown in Fig. 5, the threshold voltage is detected between nodes *a* and *c*, and the potential is added to the data voltage during the writing stage (see Fig. 6).

These simulation results are consistent with the explanation of the principle.

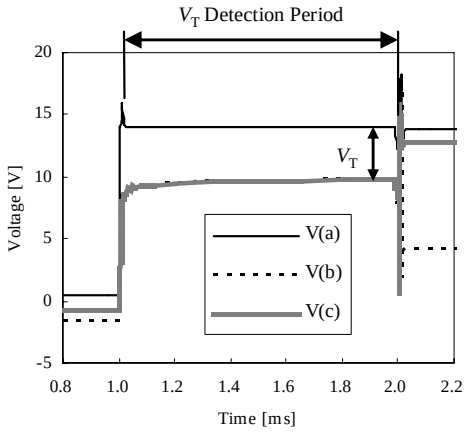

Figure 5. Simulation result for proposed pixel circuit in a subframe

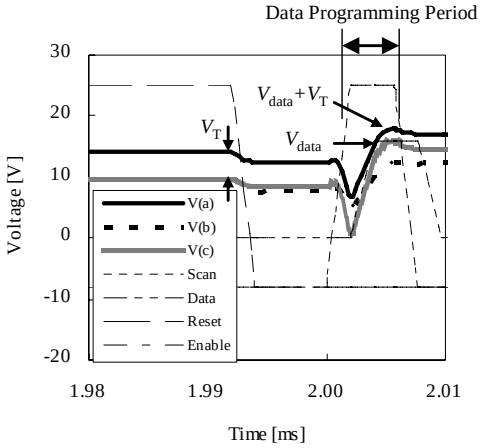

Figure 6. Simulation result for proposed pixel circuit around the programming period

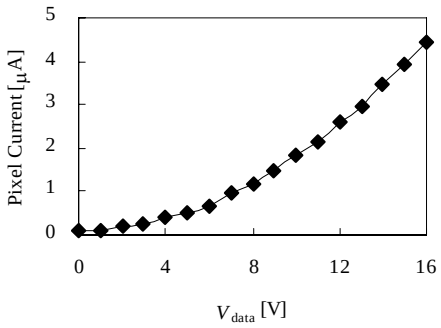

Figure 7. Dependence of the pixel current on V_{data}

We also have simulated the dependence of the pixel current on the data voltages, and the result is shown in Fig. 7. It indicates that the maximum current is 4.5 μA for V_{data} = 16 V and that a large-sized AM-OLED TV is

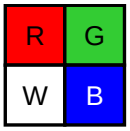

Figure 8. Suitable pixel design for the shared pixel circuit

achievable with a combination of the high-performance white OLED [4], typical LCD color filter, and the optimization of the driving wave form in Fig. 3.

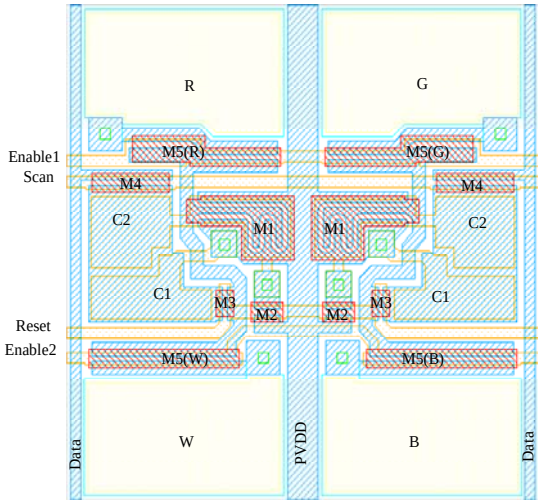

Figure 9. Example of the pixel layout for MOP = 2. Pixel size is 369 × 369 μm^2

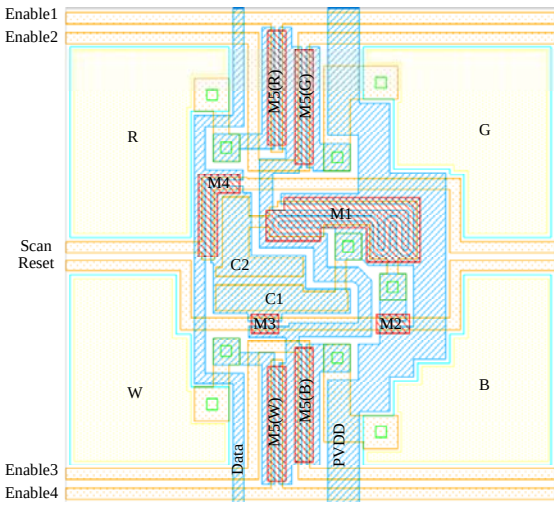

Figure 10. Example of the pixel layout for MOP = 4. Pixel size is 369 × 369 μm^2

Example of Pixel Layout

The proposed circuit is suitable for a-Si TFT backplane, a high-performance white OLED [4], and the 2 × 2 four subpixel configuration (see Fig. 8). Figures 9 and 10 are examples of the pixel layout for MOP = 2 and 4, respectively. The dimension of the transistors and capacitors are listed in Table 1. The aperture ratio for both MOP = 2 and MOP = 4 is 36.0%, but the duty ratio for MOP = 4 is one-half of that for MOP = 2. This means that the peak current for MOP = 4 is at least two times larger than that for MOP = 2, so we can expect a longer lifetime for OLED devices by using the MOP = 2 design.

Conclusions

The previously reported pixel compensation circuits are theoretically compensating for the deviation of the threshold voltage of the TFTs, but they are not applicable to a shared pixel compensation method. The novel pixel circuit that we propose is efficient enough to compensate for the deviation of the threshold voltage of the TFT, and we have also achieved a reduction of the number of electrical parts per pixel: three TFTs and one capacitor per subpixel for MOP = 2, and two TFTs and one-half of a capacitor per subpixel for MOP = 4.

Acknowledgements

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