New Feedback, Constant Current, and Constant Drain Bias Test for Amorphous-Silicon Backplane of Active-Matrix Organic Light-Emitting Diode Displays

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Abstract: *A new feedback constant current bias and temperature stress (feedback CC-BTS) test and its system are proposed and were developed to characterize the instability issue of amorphous-silicon TFTs during compensation to enable amorphous-silicon-driven active-matrix organic light-emitting diode displays (AMOLEDs). By using this system, it is possible to apply to TFTs mostly the same stress as occurs in pixel circuits with compensation schemes and can predict accurate display lifetime compared with the conventional lifetime estimation.*

Keywords: Amorphous-silicon; TFTs; AMOLEDs; threshold voltage; instability; feedback CC-BTS.

Introduction

AMOLEDs have a great potential for high image quality and low manufacturing cost compared with AMLCDs. Recently, AMOLEDs using a-Si:H TFTs were demonstrated; these are essential technologies for large-size displays, especially TVs, and they have low manufacturing cost [1,2,3]. However, the instability of a-Si:H TFTs is yet a fundamental issue. What is required is not only the compensation circuit but also further understanding of the instability for realization of TV applications, which require high image quality and long lifetimes.

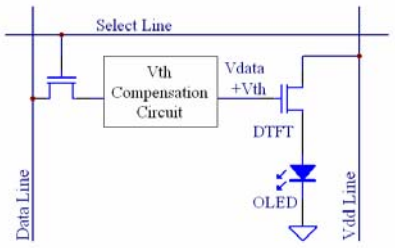


Figure 1. Diagram of a pixel circuit with compensation schemes.

Figure 1 shows a diagram of a pixel circuit with compensation schemes of AMOLEDs. The circuit works to program vdata + Vth on the gate node of DTFT and the drain current of DTFT to supply to OLED is dependent on the Vth shift. Therefore, DTFT is stressed under an almost constant current. The drain-source voltage of DTFT is mostly constant. Strictly speaking, the voltage rise of OLEDs is observed when they age. On the other hand, a-Si:H TFTs are used as switching devices and are stressed under constant voltage in AMLCDs. The instability of a-Si:H TFTs has been studied predominately under constant voltage conditions to characterize a-Si:H TFTs as switching devices [4,5,6]. Hence, it is necessary to understand the instability of a-Si:H TFTs under constant current and constant drain bias conditions in order to characterize a-Si:H TFTs as driving devices in pixel circuits with compensation schemes.

In this paper, we propose the feedback CC-BTS system that enables one to apply to TFTs mainly the same stress as that which occurs in pixel circuits with compensation schemes. Drain current is kept at constant by OP-AMP, which controls gate node with constant drain bias.

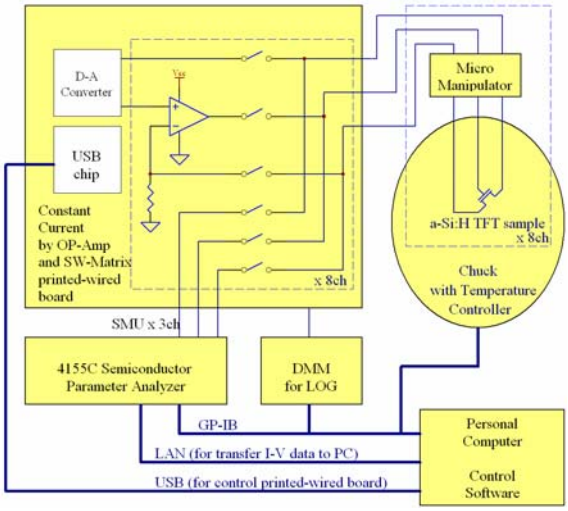


Figure 2. Block Diagram of the CC-BTS system.

Experimental

Figure 2 shows the block diagram of the feedback CC-BTS system consisting of a semiconductor parameter analyzer 4155C, a printed wired board (PWB), a digital multimeter, a thermal chuck, and a personal computer to control the system and to save the data from the 4155C and the digital multimeter. The PWB has an 8-channel constant current controlled by the OP-Amp, which can set current, drain voltage controlled by a D-A converter, and an 8-channel multiplexer for I-V measurement in sequence. It is important for the precise measurement to reduce the leak current in the PWB. To reduce the leak current of the sensitive signals,

1. high isolation resistance of mechanical relay: 10^{14} Ω<;
2. Teflon® standoff;

3. either add the guards at the same voltage as the signals or replace by coaxial cable, which is at the same voltage outside as the signal is inside;

are employed. As a result, the leak current is suppressed less than 5 pA.

The feedback constant current included in the PWB, shown in Figure 3 as a simple diagram, differs from the well-known gated-diode constant current shown in Figure 4 [8]. Although drain voltage is kept at constant voltage in the feedback constant current, drain voltage rise is observed in the gated-diode constant current. Therefore, it cannot apply the same stress to TFTs that occurs in pixel circuits with compensation schemes.

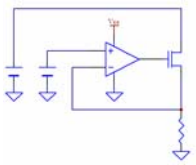


Figure 3. Feedback constant simple diagram.

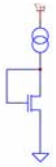


Figure 4. Gated diode simple diagram.

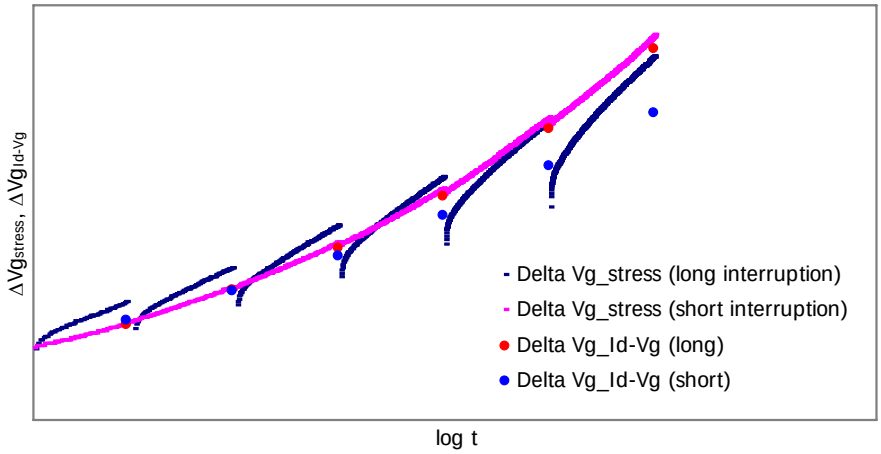


Figure 5. The feedback CC-BTS-induced ΔVg_{stress} and $\Delta Vg_{Id\text{-}Vg}$ as a function of the stressing time under various interruption times. The short interruption time for the Id-Vg measurement is 10 times shorter than the long interruption time. $\Delta Vg_{stress} = Vg_{stress}(t) - Vg_{stress}(0)$, $\Delta Vg_{Id\text{-}Vg} = Vg_{Id\text{-}Vg}(t) - Vg_{Id\text{-}Vg}(0)$, $Vg_{Id\text{-}Vg}$ = Vg at stress current.

Results and Discussion

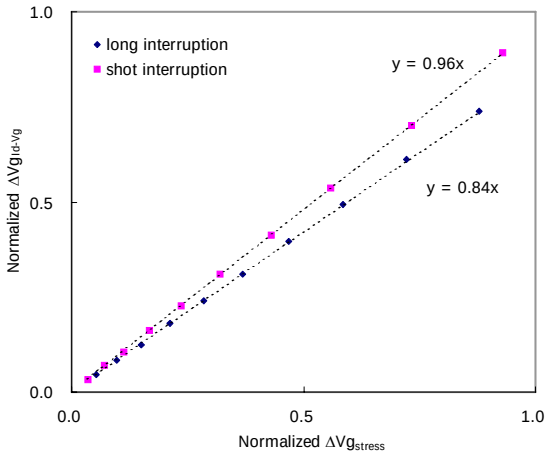
We have performed feedback CC-BTS measurements in the saturation operation regime by the developed system while monitoring the gate node voltage simultaneously, which controls the drain current as constant by a feedback loop, as shown in Figure 4. The stressing was interrupted at pre-established time intervals and Id-Vg transfer characteristics were measured. The same voltage was applied to the drain node in the Id-Vg measurement as was applied in stressing during Id-Vg measurements.

Figure 6 shows normalized $\Delta Vg_{Id\text{-}Vg}$-normalized ΔVg_{stress}. ΔVg_{stress}'s in Figure 6 are ΔVg_{stress}'s just before the interruption for Id-Vg transfer characteristics measurement. The slope of $\Delta Vg_{Id\text{-}Vg}$- ΔVg_{stress} is 0.96 in the short interruption, and in contrast, 0.84 in the long interruption. The short interruption is the modified software sequence during the interruption. The short interruption is 10 times shorter than the long interruption. Although the slope should be 1 in the idealized situation, in the actual measurements, the difference between $\Delta Vg_{Id\text{-}Vg}$ and ΔVg_{stress} is observed because of the charge relaxation from interfacial trapping levels in the interruption time [6]. It is important to suppress the effect of relaxation for characterization ΔVth as a function of the stressing time. The system puts into place that the slope of $\Delta Vg_{Id\text{-}Vg}$- ΔVg_{stress} is 0.96.

Figure 7 shows normalized ΔVth-normalized $\Delta Vg_{Id\text{-}Vg}$. ΔVth = Vth (t) – Vth (0). Vth is extracted by extrapolating a straight-line fit using plot √Id-Vg for the slope at max δ(√Id)/δ(Vg) to the gate voltage axis. The slopes of ΔVth-$\Delta Vg_{Id\text{-}Vg}$ are 1.08 in the short interruption and 1.09 in the long interruption. The slopes are independent of the interruption time. It appears that the relaxation impact is negligibly small. Because max δ(√Id)/δ(Vg), Vth is extracted from this, consists of a small number of measured points per Id-Vg measurement, and takes less than 2 s to measure these points. The time to measure these points is significantly short compared with the interruption time. The slopes are independent of the stressing time as well. This result indicates that it is possible to understand ΔVth as a function of the stressing time from,

1. ΔVg_{stress};
2. an Id-Vg measurement before starting feedback CC-BTS measurement to understand the ratio of $\Delta Vth/\Delta Vg_{Id\text{-}Vg}$;

and the stressing interruptions for Id-Vg measurement, which may cause inaccuracies as a result of charge

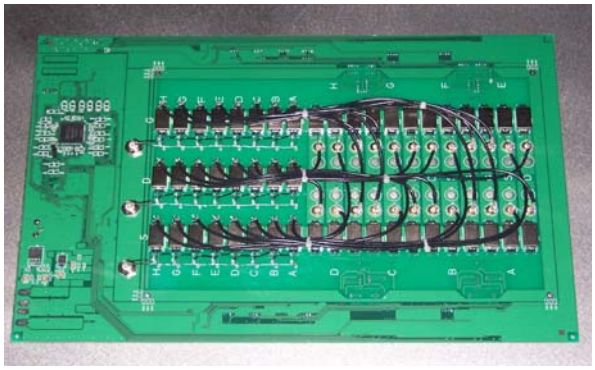


detrapping in lifetime prediction, are not required at pre-established time intervals by using this system.

Figure 6. Normalized Δ $Vg_{Id\text{-}Vg}$-normalized ΔVg_{stress}. The dashed lines are straight-line fit, respectively.

Conclusion

A new feedback constant current bias and temperature



stress (feedback CC-BTS) test and its system are proposed and developed, as shown in Figure 8. It is a powerful tool used to understand the detail of instability of a-Si:H TFTs as driving devices for AMOLEDs.

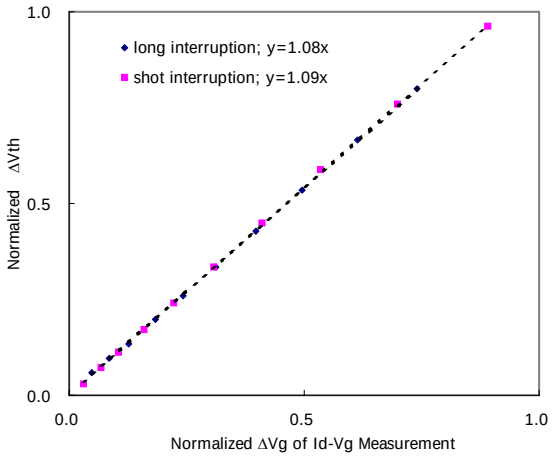


Figure 8. The printed wired board of the feedback CC-BTS system

Figure 7. Normalized ΔVth-normalized ΔVg_{stress}. The dashed lines are straight-line fit respectively.

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