Modeling of the Threshold Voltage Shift Dependency on the Drain Bias in Amorphous Silicon Thin-Film Transistors in Active Matrix Organic Light-Emitting Diode Displays

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Abstract: *A theoretical model to interpret appearances of the threshold voltage shift in hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFT's) is developed to better understand the instability of a-Si:H TFT's for the driving transistors in active matrix organic light-emitting diode (AMOLED) displays. This model assumes that the defect creation is proportional to the carrier density in a-Si:H, leading to the defect density that varies along the channel depending on the bias conditions. The model interprets a threshold voltage shift dependency on the drain stress bias. The threshold voltage shift stressed with a gate bias in the saturation condition will be 2/3 of that stressed in the linear region even with the same gate bias stress, and can be even smaller when stressed in deeper saturation region.*

Keywords: Active matrix organic light-emitting diode; amorphous silicon thin film transistor; threshold voltage shift.

Introduction

Hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFT's) are successful switching devices in the active matrix (AM) liquid crystal display (LCD) industry. Recently, as the efficiency of organic light-emitting diodes (OLEDs) has been improved, they have been investigated as analog devices for the use of driving TFT's in AMOLEDs [1,2]. Instability of the threshold voltage is a major issue in such applications.

It is widely accepted that the direct cause of the threshold voltage shift is the creation of meta-stable states in a-Si:H and the charge trapping in the gate insulator [3]. The deep-level defect creation is recognized as dominant under relatively low gate-bias [4], which is our interest for driving AMOLEDs. In the defect-pool model, the rate of the defect creation is proportional to the density of charge induced in the conduction tail band [3]. It is reported experimentally that a-Si:H TFT's suffered from a gate-bias stress shows smaller threshold voltage shift when driven in the saturation region than in the linear region [5].

Karim et al. explained the drain-bias dependence of the threshold voltage shift from the gate-to-drain bias dependence of the charge induced in the channel [6]. They described the threshold voltage shift dependence on the drain bias as a function of gate-to-source bias, gate-to-drain bias and the threshold voltage. They derived that the V_{th} shift in the saturation region was 2/3 of that in the linear region. It is easily associated that the charge induced in a-Si:H when the drain bias is applied is not uniform along the channel because of the potential distribution from the source to drain, resulting in various defect distribution along the channel [7].

In this work, the density of electrons in a-Si:H is analytically calculated to determine the spatial distribution of the created defects in a-Si:H, assuming the defect creation is proportional to the electron density. The appearance of the threshold voltage shift is calculated from the defect distribution to derive the threshold voltage shift dependency on the drain bias.

Modeling and Calculations

The charge induced in the channel consists of free electrons induced in the extended states and the localized electrons trapped in the acceptor-like tail states and the acceptor-like deep states. The density of the tail states can be approximated exponentially dependent on energy below the conduction band edge, E_c. The extended states associated with the short-range order of a-Si:H become dominant above E_c.

For simplicity, here we assume that the density of states converges to a constant N_t when $E>E_c$ as shown in Fig.1, that the electrons trapped in the states equally contribute to the defect creations, and that the ambient temperature is the same as the tail states characteristic temperature. The deep sates initially exist are omitted here, since they will increase the initial threshold voltage, but will have no influence on the shift of the threshold voltage attributed to the degradations. The density of states may depend on the square root of energy above E_c [8], but the probability of occupation above the E_c decreases

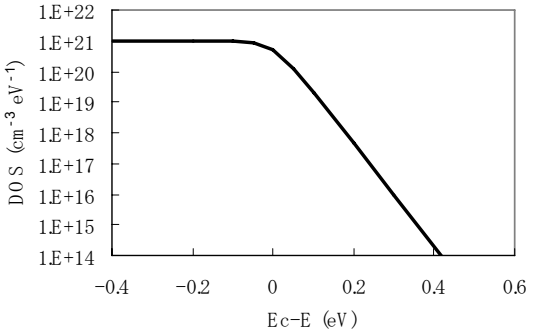

Figure 1 The density of states (DOS) of a-Si:H TFT assumed in this work.

exponentially on energy, therefore, the electrons induced in the higher states is relatively minor. In the equilibrium states, the probability of occupation of the acceptor-like tail states is given by the Fermi-Dirac statistics. Integrating the product of the density of states and the probability of occupation yield the density of electron, *n*,

induced in a-Si:H as a function of the potential, ϕ, in a-Si:H.

$$n(\phi)=\int \frac{N_t}{1+\exp\left(\frac{E_c-E}{kT}\right)}\cdot\frac{1}{1+\exp\left(\frac{E-E_f-q\phi}{kT}\right)}dE$$

$$=\frac{N_t\left(q\phi+E_f-E_c\right)}{1-\exp\left(-\frac{q\phi+E_f-E_c}{kT}\right)}$$

$$\approx N_t\left(q\phi+E_f-E_c\right)\qquad \left(q\phi+E_f\geq E_c\right) \quad (1)$$

where N_t is the density of the tail states when $E=E_c$, E_f is the Fermi level, k is the boltzman constant, and T is the temperature.

As the thickness of a-Si:H layer in TFT's is usually less than 1/10 of the channel length, the electric field to the channel depth is small compared with that along the channel length. Here, we assume that the most of the charge induced in a-Si:H determines the electric field perpendicular to the channel. It is convenient to distinguish the electrons trapped in the deep states from the others to discuss the amount of threshold voltage shift associated with them. Solving the one-dimensional Poisson's equation with Eq.(1), we obtain

$$n(x,y)+\Delta N_d(x,y)$$
$$=\frac{C_{ox}}{q}\left(V_g-V_{thi}-V_{bc}(y)\right)\exp\left[-q\sqrt{\frac{N_t}{\varepsilon}}x\right] \quad (2)$$

where ΔN_d is the density of the deep states created in a-Si:H by the bias-stress, C_{ox} is the gate capacitance, V_{thi} is the initial threshold voltage defined as $V_{thi}=V_{fb}+\left(E_c-E_f\right)/q$ with the flat-band voltage V_{fb}, and $V_{bc}(y)$ is the back-channel potential. ε is the permitivity of a-Si:H.

Equation (2) indicates that the carrier is mostly concentrated near a-Si:H/gate-insulator interface with the specific depth $x_0=1/q\sqrt{N_t/\varepsilon}$ ~10[Å], when N_t~10^{21}[$cm^{-3}eV^{-1}$]. Therefore, the defect creation mainly occurs at the interface and is locally interpreted as the increase of the flat-band voltage, Δv_{fb}, inducing the charge trapped in the deep states.

$$\Delta v_{fb}(y)=\frac{q}{C_{ox}}\Delta N_d(x,y) \quad (3)$$

Because we assume the rate of the deep state creation is proportional to the density of the electrons as is in the defect-pool model [3],

$$\frac{dN_d}{dt}=\frac{n(x,y)}{\tau} \quad (4)$$

where τ is the time constant of the defect-creation reaction, considered as a function of stress time, proposed to have the power dependency on time reflecting the dispersive diffusion of the hydrogen in the reaction [4].

The electric field along the channel near the interface can be determined self-consistently [9] using the specific depth x_0 as

$$\frac{\partial\phi(x_0,y)}{\partial y}=-E_y(x_0,y)=\frac{I}{\mu q\int n(x,y)dx} \quad (5)$$

where μ is the channel mobility of electrons. The back channel potential $V_{bc}(y)$ is determined to be consistent with the surface potential $\phi(x_0,y)$ in Eq.(5). From Eq.(2)-(5), we obtain the density of charge induced in a-Si:H as

$$n(x,y)=\frac{C_{ox}}{q}\left(V_g-V_{thi}\right)$$
$$\times\exp\left[-q\sqrt{\frac{N_t}{\varepsilon}}x\right]\sqrt{1-2\eta(1-\eta)\frac{y}{L}}\cdot\left(1-\exp\left[-\int\frac{dt}{\tau}\right]\right) \quad (6)$$

where

$$\eta=\frac{V_d}{V_{dsat}}=\frac{V_d}{V_g-V_{thi}} \quad (7)$$

with V_{dsat} as the saturation drain voltage.

Figure 2 indicates that the induced carrier by Eq.(6) and, therefore, the defect created, are concentrated near the a-Si:H/gate-insulator interface with the spatial distribution of square-root along the channel. The threshold voltage shift, dV_{th}, appears in IV characteristics of a-Si:H TFT as the integration of the flat band voltage shift Δv_{fb} along the channel. Using Eqs. (3) and (4), the threshold voltage dependence on the drain-bias is obtained with

$$\frac{dV_{th}}{dV_{th0}}=\frac{2}{3}\cdot\frac{2-2\eta+\eta^2}{2-\eta} \quad (8)$$

where dV_{tho} is the threshold voltage shift when stressed in the linear condition, where the drain-to-source bias is zero.

Equation (8) gives 2/3 at $V_d=V_g-V_{thi}$. The equation gives the same threshold voltage suppression at the saturation condition as is calculated by Karim et al. [5]. This is not surprising, as we eventually applied the same approach to determine the potential along the channel in Eq.(5).

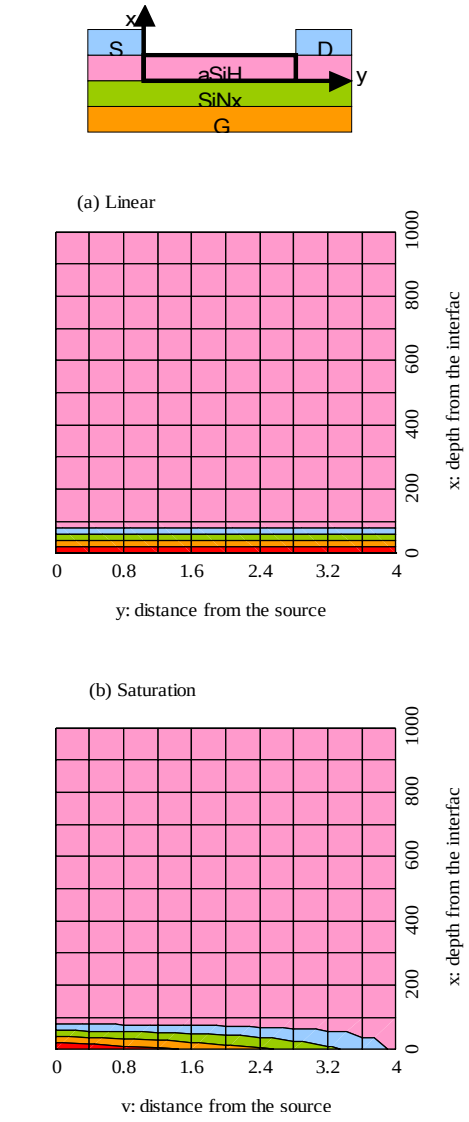

Figure 2 The electron distribution in channel (a) in the linear region, V_d=0, and (b) in the saturation region, V_d=V_g-V_{thi},

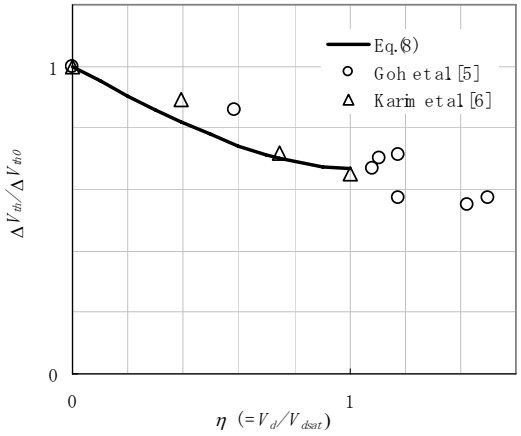

Figure 3 V_{th} shift dependence on the drain bias voltage: plot of Eq.(8) with experimental data referenced from [5, 6

Figure 3 is the plot of Eq.(8) with experimental results reported by other groups [5,6]. Eq.(8) shows a good agreement with the data. The data from Ref.[5] implies the threshold voltage shift in deeper saturation region could go down even smaller. The induced electron does not increase any more when the drain bias is applied beyond the saturation drain voltage, V_{dsat}, since the electric field along the current path concentrates near the drain to consume the extra voltage. However, the spatial concentration of the induced electron along the channel squeezed toward the source side because of the charge vacancy near the drain to afford the concentrated electric field. Therefore, the defect creation hardly occurs at this region, and the threshold voltage shift in deeper saturation region becomes even smaller.

Conclusions

We theoretically derived the flat band voltage shift distribution in the channel attributed to the deep-states defect creation when the gate and the drain bias applied to a-Si:H TFT's and calculated the appearance of the threshold voltage shift in TFT IV characteristics as a function of the drain voltage. The analysis implies that the threshold voltage shift of a-Si:H TFT's driven with various drain biases appears largest at the linear condition and becomes smaller with higher drain bias, down to 2/3 at the saturation condition, which shows good agreement with experimental data reported by others. It could go even smaller when driven in the deeper saturation region.

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