Impact ionization model for kink effect in Poly-Si TFTs for display devices

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Abstract: *The last decade has witnessed a tremendous progress in the field of flat panel displays using polycrystalline silicon thin-film transistors (TFTs)-LCDs. But as we know that polysilicon TFTs suffers from several undesired effects and kink effect is one of them. In this paper kink effect in poly-Si TFTs is studied by developing an impact ionization model using a quasi-two-dimensional approach. It is found that lower gate voltage results in a more prominent kink effect. It is also observed that the drain current increases at higher drain voltage which is due to the increase in carrier density due to the impact ionization. In order to verify the validity of the developed model, the computed variations are compared with the experimental results and the agreement found is quite reasonable.*

Introduction

It is well known that the output characteristics of poly-Si TFTs exhibit an anomalous current increase at high drain voltages, often called "kink effect" [1]. This effect results in an increase of the output conductance and, therefore, increases, in digital circuits, the power dissipation and slightly degrades the switching characteristics, while, in analogue circuit applications, it reduces the maximum attainable gain as well as the common mode rejection ratio. Since, the poly-Si TFT circuits employ relatively higher supply voltages; the electric field in the saturation region tends to be very high. So it is important to study and develop the model which remains valid in the saturation region.

To achieve a physical insight on the kink effect several authors have performed two-dimensional (2-D) numerical simulation [1-2]. In particular, this effect is originated by impact ionization at the drain end of the channel, where the electric field is larger. In this study kink effect in poly-Si TFTs is studied by using a quasi-two-dimensional approach.

Theory

Assuming that polysilicon material used in the channel of TFTs is composed of a linear chain of identical silicon crystallites (grains) having a grain size of D_G, separated by the regions with high density of impurities called grain boundaries (GBs) which are straight and perpendicular to the carrier flow. It contains N_T (cm^{-2}) number of traps located at energy E_T with respect to the intrinsic Fermi level.

The drain current for the output characteristic of a poly-Si TFT is given by

$$I_D = (\mu_{eff} ZC_{ox}/D)\,[(V_G - V_T)V_D - V^2_D/2\,] \qquad (1)$$

where Z/D is the channel width to length ratio and μ_{eff} is the effective carrier mobility in the channel of a poly-Si TFT.

On the basis of the quasi-two-dimensional approach a Gauss box is defined from the position where the electron starts to travel at a saturated velocity to the drain edge in the whole thin film region. Considering the electron density n and the average trapped charge density N_T/D_G and N_A in the Gauss box as shown in figure 1, one obtains

$$\mathbf{D}.\mathbf{dl} = -q\int_0^{y}\int_0^{\gamma t_i} (N_T/D_G + n + N_A)\,dx\,dy$$
$$= \int_0^{\gamma t} \varepsilon_s\,[E_y - E(0)]\,dx - \int_0^{y}\varepsilon_{ox}\,E_x\,dy \qquad (2)$$

where **D** is the electric displacement vector perpendicular to the path, γ is the modeling parameter, ε_{ox} is the permittivity of oxide and E(0) is the *y* component of the electric field at the pinch-off point (*y*=0), which is the location where the channel potential reaches saturation. In the channel region of poly-Si TFT below SiO_2 layer, the *x* component of the electric field is

$$E_x = C_{ox}[V_G - V_T - V(y)]/\varepsilon_{ox} \qquad (3)$$

where V(*y*) is the channel potential and E_y is the *y* component of field at location *y*.

From eq.(2)-(4) one obtains:

$$E_y - E(0) + (C_{ox}/\varepsilon_s\gamma t_i)\int_0^{y} V(y)\,dy = [(-q/\varepsilon_s)/\,(N_T/D_G + N_A) + (C_{ox}/\varepsilon_s\gamma t_i)\,V_{SAT}]\,y \qquad (4)$$

Differentiating both sides of eq. (6) and from eqs. (2) and (3), one obtains

$$d^2\,V(y)/dy^2 - (C_{ox}/\varepsilon_s\gamma t_i)V(y) = (q/\varepsilon_s)\,(N_T/D_G + N_A) - (C_{ox}/\varepsilon_s\gamma t_i)\,V_{DSAT} \qquad (5)$$

Solving the differential equation we get

$$V(y) = C_1\exp\{\delta\, y\} + C_2\,\exp\{-\delta y\} + [V_{DSAT} - (q/\varepsilon_s\delta^2)(N_T/D_g + N_A)] \qquad (6)$$

where $\delta = \sqrt{(C_{ox} / \varepsilon_s \gamma t_i)}$

Now using the boundary conditions: at $y = 0$, $V(y) = V_{DSAT}$ and $E(y) = -Ec$ (critical electric field) we get

$C_1 = 0.5 [(q / \varepsilon_s \delta^2)(N_T / D_G + N_A) + Ec / \delta]$ and
$C_2 = 0.5 [(q / \varepsilon_s \delta^2)(N_T / D_{gG} + N_A) - Ec / \delta]$

At drain, $V(d_s) = V_D$, From eq (6), the length of the post-saturation region is:

$$d_s = (1/\delta) \ln \{[V_D - V_{DSAT} + (q / \varepsilon_s \delta^2)/(N_T / D_G + N_A)] + \sqrt{\{[V_D - V_{DSAT} + (q / \varepsilon_s \delta^2)/(N_T / D_G + N_A)]^2 - 4 C_1 C_2\}}/2 C_1 \qquad (7)$$

The current as a result of impact ionization (avalanche) is [3]

$$I_{av} = I_{DSAT} (M_{av} - 1) \qquad (8)$$

where M_{av} is the avalanche multiplication factor, which is related to the lateral electric field in the device by the electron impact ionization coefficient $[\alpha \exp(-\beta / E_y)]$. By integrating the electron impact ionization factor throughout the post-saturation region, the avalanche multiplication factor is obtained as

$$M_{av} = \int_0^{d_s} [\alpha \exp(-\beta / |E_y|)\, dy = \int_{V_{DSAT}}^{V_D} [\alpha \exp(-\beta / |E_y|)/|E_y|\, dv \qquad (9)$$

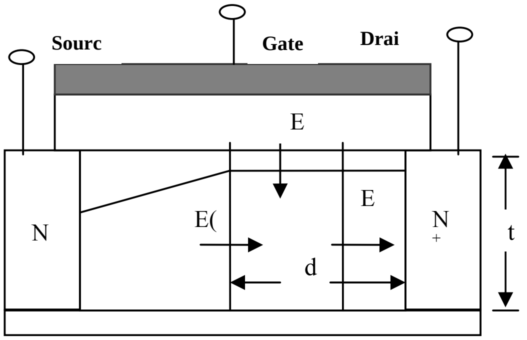

Figure 1: Cross section of the inversion-type poly-Si TFT used for impact ionization modeling.

From eq (5), the lateral electric field is given by

$$E_y = \{\delta^2 V(y)^2 + [(2q / \varepsilon_s)(N_T / D_G + N_A) - 2\delta^2 V_{DSAT}] V(y) - [(2q / \varepsilon_s)(N_T / D_G + N_A) V_{DSAT} - \delta^2 V^2_{DSAT} - E_c^2]\}^{1/2} \qquad (10)$$

At drain, the electric field can be written as:

$$E_{yd} = \{\delta^2 V_D^2 + [(2q / \varepsilon_s)(N_T / D_G + N_A) - 2\delta^2 V_{DSAT}] V_D - [(2q / \varepsilon_s)(N_T / D_G + N_A) V_{DSAT} - \delta^2 V^2_{DSAT} - E_c^2]\}^{1/2} \qquad (11)$$

From eq (9) and (11), the electron multiplication factor becomes

$$M_{av} \approx 1 + (\alpha/\delta)(E_{yd} / \beta - E^2_{yd} / \beta^2 + E^3_{yd} / \beta^3)\, e^{-\beta / E_{yd}} \qquad (12)$$

The drain current, which is composed of the avalanche current (I_{av}) and I_{DSAT}, with kink effect becomes

$$I_D = M_{av} I_{DSAT} \qquad (13)$$

For small values of V_D, kink effect is negligible; hence $M_{av} = 1$.

Discussion

The parameters used in the analysis are shown in Table 1. Figure 2 shows the computed I_D-V_D characteristics of poly-Si TFT for different gate voltages and shows the effect of impact ionization, where a lower gate voltage results in a more prominent kink effect. This is attributed to the fact that the maximum electric field decreases with increase in the gate voltage (V_G) and also the intensity of carrier generation decreases with increase in the V_G . This is because the lateral component of the electric field at the drain end, which is responsible for the generation of charge carriers, decrease with increasing gate voltage, for a constant drain voltage. It is also observed that the drain current increases at higher drain voltage which is due to the increase in carrier density due to the impact ionization.
In order to verify the validity of the developed model, the computed variations at $V_G = 7$ volt are compared with the experimental results of L.Mariucci *et. al.*[4]. A very good agreement has been obtained between experimental results and computed values.

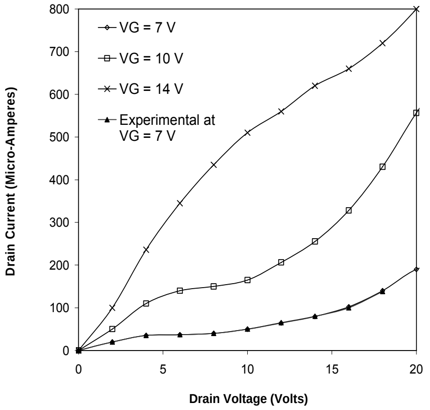

Figure 2: I_D-V_D characteristics of poly-Si TFT for different V_G. Triangles are experimental results.

Table1: Parameters of the poly-Si TFT used in the analysis of kink effect

Symbol		Value
1.	E_c	9.0×10^{4} V/cm
2	γ	0.9
3	α	2.0×10^{6} cm^{-1}
4	β	1.46×10^{6} V/cm
5	v_{sat}	6.0×10^{6} V/cm
6	C_{ox}	354 μF/m^{2}
7	t_i	200 nm
8	N_T	2.0×10^{12} cm^{-2}
9	D_G	100 nm
10	N_A	10^{16} cm^{-3}
11	ε_s	104.43×10^{-12} C^{2}/Nm^{2}

References

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