Improving the performance of poly–silicon thin film transistor for switching and driver circuitry

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Abstract: *With the growing interest in the flat panel displays, the poly–Si TFT have emerged out as a suitable candidate to meet with both display and driver capability. These advances have led to research motivation towards poly–Si TFT to enhance its performance and suppress its demerits such as high threshold voltage, low field effect mobility, low drive current, kink effect etc. In this work, we have proposed surrounding gate (SUG) geometry for poly–Si TFT, and its device characteristics are compared with its single gate (SG) and double gate (DG) counterparts. Extensive simulations have been done to study SUG performance and its merit over regular structures. The obtained results reflect the up–gradation of device performance by reducing device threshold voltage, and thus, power consumption for switching applications. The drain current performance has also been improved, thereby finding feasibility in driver circuitry applications.*

Keywords: Poly–silicon TFT; Surrounding gate, Kink effect.

Introduction

This article describes about the prevalent floating–body effects in the poly–crystalline silicon thin film transistors (poly–Si TFTs), which are triggered by impact–ionization charging of the film body, and is commonly known as the 'kink' effect [1–2]. This kink effect is not harmful, but is undesirable because of the abnormality it creates, which can be detrimental in complementary–metal–oxide–semiconductor (CMOS) circuits for analog applications, three–dimensional (3–D) device integration, high density static random access memories (SRAMs) and liquid flat displays (LFDs) [3–7]. It causes current overshoots [8] in the devices, and thus, is difficult to model, to implement in circuit simulators [9] and therefore, must be constrained. From the preceding considerations, the mechanism of the kink effect can be explained as; due to device depletion, the holes are rushed down to substrate region and these accumulated holes raises the electrostatic potential in the substrate region, which increases the drain current. This increased drain current further produces many more holes through the avalanche process. These processes act as positive feedback for an abrupt increase in the drain current at kink voltages. The accumulated holes in the substrate region, however, get reduced with the increase in the recombination process rate, which acts as a negative feedback for the current increase. Therefore, kink effect can also be explained as an abrupt increase in the drain current, which is motivated by a positive feedback, and is then suppressed by a negative feedback, because of an abrupt increase in the current value.

It is interesting to question why avalanche generation effects are much larger in the poly–Si TFTs, than in single–crystal devices. Poly–silicon devices show much larger avalanche effects because the space charge is primarily determined by trapped carriers and not by free carriers. These traps occur due to the presence of grain–boundaries in the poly–Si film. Furthermore, the dependence of the kink effect upon recombination processes is also occurring via traps. Higher avalanche multiplication can be enlightened as; in the sub–threshold regime, the current in single–crystalline silicon device falls–off much more rapidly with decreasing gate voltage than in a poly–Si TFT, because the latter contains traps that reduce the sub–threshold slope. Hence, the poly–Si TFT has a higher carrier concentration in the sub–threshold regime, causing higher avalanche generation. The kink effect is a very serious problem in poly–Si TFT, because it deteriorates the output characteristics both in digital and in analog circuit applications (e.g., reduced noise margins and available voltage gain) of poly–Si TFT, and reduces the poly–Si TFT amplifier gain [10]. In addition, the kink effect causes the avalanche induced short–channel effect, which places the limitation on scaling down the device size [11]. Although the published studies of these effects involve only bulk–like (partially depleted) silicon–on–insulator (SOI) devices, they can occur in fully depleted devices [12] also associated with the parasitic bipolar junction transistor (BJT) action.

To overcome this kink effect or to suppress its effect on the device characteristics, different gate–engineered structured poly–Si TFT have been well examined in this work. The simulated structures comprises of conventional single gate (SG) poly–Si TFT, double gate (DG) poly–Si TFT and surrounding gate (SUG) poly–Si TFT. The impact of the alteration in the gate geometry is well shown on the device characteristics such as threshold voltage and drain current.

The introduction of vertical surrounding gate (SUG) MOSFETs has witnessed higher packing densities in memories and logic chips along with enhanced performance [13]. Thus, the suppression or delayed response of kink current together with above said merits will serve poly–Si TFT as a useful device for upcoming device and circuit applications.
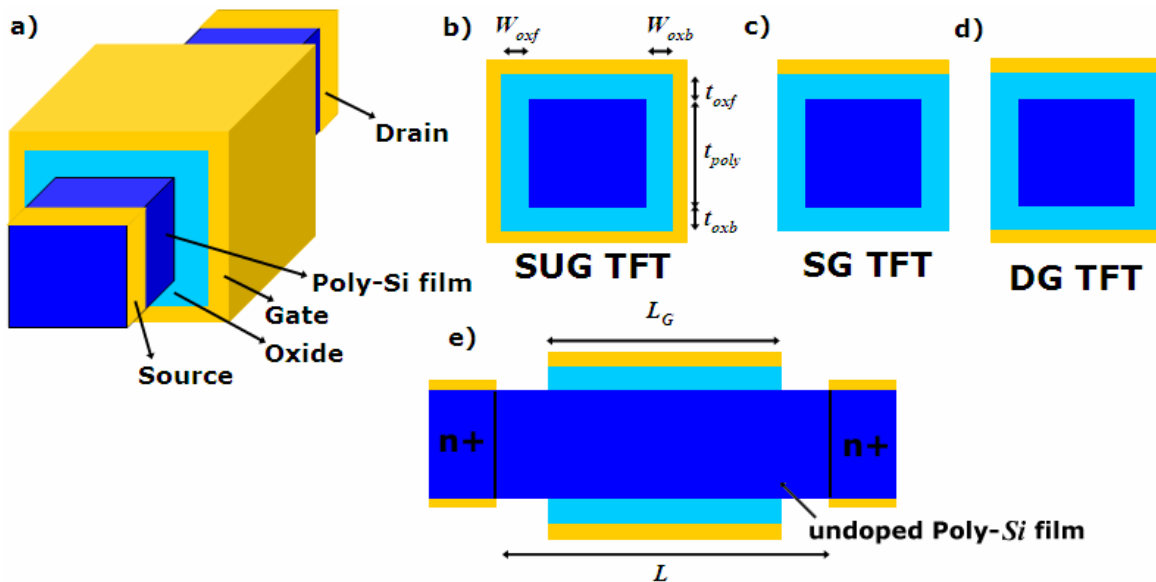
Figure 1. a) Schematic diagram of poly–*Si* thin film transistor. b) Cross–sectional view of SUG TFT. c) Cross–sectional view of SG TFT. d) Cross–sectional view of DG TFT. e) Cross–sectional view along the device length.

Simulation and Discussion

Simulation

The work done encompasses extensive simulations performed using the ATLAS simulator [14]. The model for the simulation of poly–*Si* devices is based on parallel electric field effect mobility model, Schokley–Read–Hall generation and recombination of carriers in trap states and Selberherr's impact ionization model. In our case, the effect of trap/defect states is incorporated using continuous density of states. The density of defect states used in the analysis is a combination of exponentially decaying band tail states and Gaussian distribution of mid–gap states. It is assumed that the total density of states comprises two tail bands (donor–like valence band and acceptor–like conduction band), and two deep level bands (acceptor–like and donor–like Gaussian distribution) [15].

Figure 1 shows the schematic and cross–sectional view of the gate–engineered poly–*Si* TFTs. The structure comprises of the gate length L_G, the channel length L equal to 0.5µm greater than the gate length in equal proportions (i.e. 0.25µm towards source–end and 0.25µm towards drain–end), t_{oxf} is the front–end oxide thickness, t_{oxb} is the back–end oxide thickness, W_{oxf} is the front–end oxide width, W_{oxb} is the back–end oxide width. The material used in the analysis comprises of aluminium as gate electrode. The source–end and drain–end contacts are surrounding electrode contacts designed across the poly–*Si* film cuboid.

Threshold Voltage

The threshold voltage (V_{th}) of the device is one of the most important parameter for circuit, device and process characterization particularly for modern devices with very small geometry and relatively low supply voltages. To maintain optimum device performance, the threshold voltage of the device is required to be studied and monitored continuously. The need for low threshold voltage device arises to save large power dissipation and to lower the supply voltage while switching to high density packing.

In our simulations, the constant current method is used to extract the threshold voltage of the device using the current criterion of $I_{ds}=10^{-8}$A, which in–turn relates to an extrinsic measurable quantity from experimental overview.
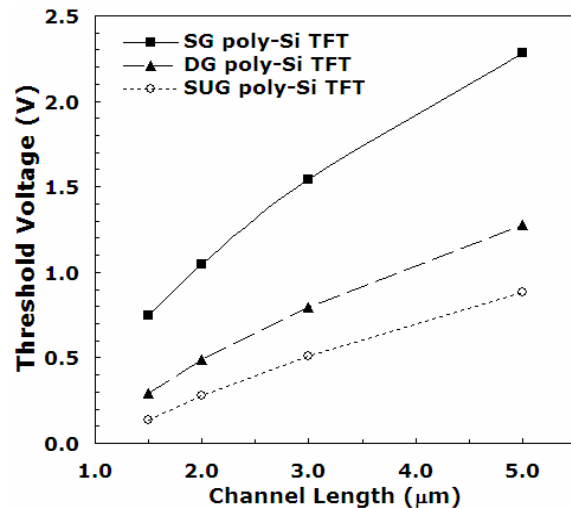

Figure 2. Variation of threshold voltage with channel length for poly–*Si* TFTs shown in Figure 1.

Threshold voltage variation with channel length for different poly–*Si* TFTs shown in Figure 1 is plotted in Figure 2. The short–channel effects (SCEs) become more pronounced with decrease in channel length, and can be realized from the figure as a roll–off in the V_{th} value. This happens due to the fact that decrease in channel length reduces the overall region to be depleted under the same bias conditions and thus, resulting in the early onset of

inversion of carriers. The curves also show the roll–off in the V_{th} value as we switch to DG TFT and further SUG TFT from SG TFT. This can be explained as; application of double–gate results in more depletion of the active film and thus, depletes the device at earlier gate voltages. Whereas, in case of SUG TFT, V_{th} value further roll–off because of the depletion due to surrounding gate in which depletion from width side also comes into picture.

Drain Current

The comparison of drain characteristics (I_{ds}–V_{ds}) of SG poly–*Si* TFT, DG poly–*Si* TFT and SUG poly–*Si* TFT in Figure 3 have shown enhancement in drain current performance for SUG structure with the same set of device parameters. This improved drain current characteristics will serve as an advantage for driver circuitry applications. The curves of SUG poly–*Si* TFT also show the delayed response of kink effect in the characteristics and thus, extending the saturation regime of the operation for higher drain voltages. Thus, SUG structure proved to be merit over regular structure with increased current driving capability, and shifting the impact ionization regime.
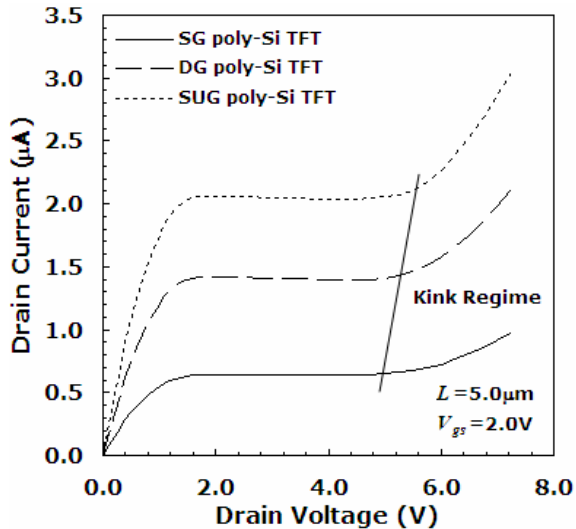
Figure 3. Variation of drain current with drain voltages for poly–*Si* TFTs shown in Figure 1.

The variation of drain current with drain voltage at different gate voltages for SUG poly–*Si* TFT is plotted in Figure 4. The increase in gate voltage shows improvement in drain current performance due to more generation of free carriers. From the curves it is seen that the kink effect shows its maximum impact at the gate voltages somewhat lower than the drain voltages, because the generation rate of holes induced by the avalanche process shows its maximum at this condition (drain voltage > gate voltage). The phenomena involved is that for high drain voltages, as the channel current is accelerated by the drain field, accelerated carriers gain enough energy to generate electron–hole pairs by impact–ionization.
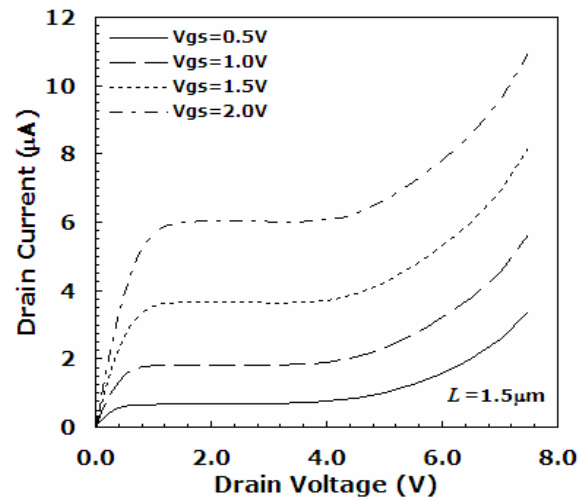
Figure 4. Variation of drain current with drain voltages for surrounding gate poly–*Si* TFT at different gate voltages.
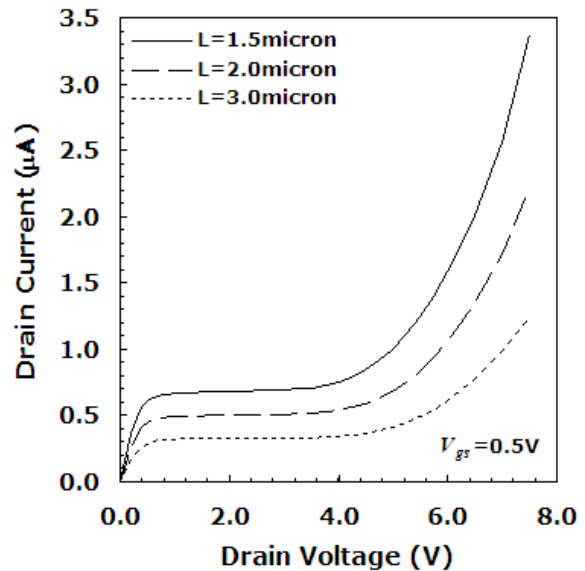
Figure 5. Variation of drain current with drain voltages for surrounding gate poly–*Si* TFT at different channel lengths.

The drain current variation with drain voltage for SUG poly–*Si* TFT at different channel length is shown in Figure 5. From the curves, it is observed that the kink effect becomes more severe as we approach short–channel lengths. This could be due to a reduction in the overall space charge. This reduction in space charge under same bias conditions influences high electric field and avalanche breakdown of device. It can be explained as; at short–channel lengths and high drain bias, the maximum electric field experienced by the carriers at the drain–end is increased. As the carriers move from source to drain, they acquire enough kinetic energy in the high field region so as to cause impact–ionization and leads to the generation of electron–hole pairs. These generated electrons are drawn towards the drain–end and cause an increase in the drain current. While the holes drift towards the substrate and get accumulated in the

substrate, the substrate potential rises till it becomes forward biased, causing further injection of electrons from the source. This added current augments the impact–ionization. This effect results in a drastic increase in the drain current at high drain voltages.

Conclusion

In this work different gate–engineered structured poly–*Si* TFT have been well examined to overcome the kink effect or to suppress its effect on the device characteristics. The results obtained show that the kink effect is more prominent at smaller dimensions. The obtained results for SUG poly–*Si* TFT reflect the up–gradation of device performance by reducing device threshold voltage and thus, power consumption for switching applications. SUG structure also proved to be merit over regular structure with improved drain current performance, and shifting the impact ionization regime, thereby finding feasibility in driver circuitry applications.

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