

Poly-Si TFT Pixel Circuits using Solid Phase Crystallized Silicon for AM-OLED Backplane

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Abstract: We report on high-performance, furnace-annealed polysilicon thin film transistors (TFT) without hydrogenation step fabricated on glass and implemented on OLED-pixel circuits. Our results show that an increase of the mobility parameter results in a higher current variations, so p-type TFT circuits are preferable. Moreover, measurements reveal that using such material threshold compensation is not able to solve entirely the non-uniformity of driving current. Nevertheless results show the possibility of using SPC-TFT as driving backplanes in the fabrication of AMOLED displays.

Keywords: active-pixel circuit; thin film transistor; current driving; solid phase crystallization (SPC); low-pressure-CVD; organic light-emitting device (OLED).

Introduction

During the last decade, active matrix organic light-emitting diode (AMOLED) displays have attracted considerable attention. Since the non-uniformity of OLED brightness is proportional to the current fluctuations flowing through the diode, a constant current must be provided by pixel drivers during each frame time. The backplane technology of choice appears to be amorphous silicon (a-Si:H) TFT by virtue of its intensive utilization in AMLCD technologies. But OLED-circuits based on a-Si:H is hindered by the temporal instability leading to an increase of current in time. Many solutions have been suggested to solve this issue using electronic compensations [1-2]. Although driving schemes improve the display luminance uniformity, inherent instability of the a-Si:H TFT involves electrical degradations with a possible reduction of the display long-term lifetime.

Another well established technology consists to obtain low-temperature polycrystalline silicon from the crystallization of amorphous deposited silicon film (LTPS) using an excimer laser annealing (ELA). However, laser technique is a highly variable process, mainly due to shot-to-shot instability and possible energy density dispersion within the beam, which produces centre-to-edge variability resulting in non-uniformity of TFT characteristics [3].

Alternative approaches such as non-laser crystallisation methods have been reported. The most famous approach is the so-called solid phase crystallization (SPC) technology that is well known to generate polysilicon with low surface roughness and good uniformity. SPC polysilicon might be an alternative solution for

AMOLED backplane. Over the last several years, there have been many studies reporting the SPC method for OLED displays. For instance in 2001, Stewart *et al.* developed a polysilicon TFT backplane based on rapid thermal processing (RTP). Here the crystallization was controlled using heating lamps at a temperature range of 677°C to 720°C [4]. Wu *et al.* fabricated in 2004 an AMOLED prototype including polysilicon films obtained from metal-induced-lateral-crystallization (MILC) [5]. More recently, Chung *et al.* also demonstrated that an AMOLED display can be achieved on large area (17-in) using a similar MILC process (SGS), where the crystallization occurred from a layer containing some nickel atoms [6]. Although these techniques provide a low surface roughness (<2nm) and relatively uniform polysilicon films, they introduce additional sensitive steps in TFT fabrication process.

Thus the conventional furnace-annealed polysilicon is probably the simplest technique to crystallize amorphous silicon films. Despite a relatively long crystallization time (~10h at 600°C), this technique offers sufficient performance to drive OLED-pixels, providing high currents with small TFT dimensions.

Yet the non-uniformity of this material have not been discussed for AMOLED displays. In this paper, as an alternative approach to the ELA or MILC techniques, we have investigated performance and emission current non-uniformity of drive-TFT fabricated using furnace-annealed polysilicon, solid phase crystallized at 600°C for 8-hours. Two simple voltage input pixel circuits arranged in an array of pixels have been fabricated and tested in DC and pulsed operations.

Experimental details

In this experiment, p and n-channel polysilicon TFT pixel circuits using a top-gate structure were fabricated on distinct glass substrates. The realization of active pixel circuits is well known now but some specificities in our developed fabrication process require a description. Figure 1. presents a schematic cross-sectional view of a pixel circuit structure.

The test circuits were fabricated as follows. The starting material was a 3-in glass substrate (Corning 1737, 0,7-mm thick). First we begin by coating one side with 250-nm thick SiO₂ insulating layer using an atmospheric-pressure-CVD (AP-CVD) system at 430°C. Polycrystalline silicon films were obtained by

crystallization of a high purity amorphous silicon layer deposited in a standard low-pressure-CVD (LP-CVD) reactor with SiH₄ source gas at a temperature of 550°C and a pressure of 90Pa. Thus, a blanket bi-layer of 150-nm thick intrinsic silicon followed by a 150-nm thick highly boron (or phosphorous) doped silicon film is deposited without interruption for the active channel layer and the S/D contacts and capacitor-electrode layer respectively. Using such method, interface between undoped and doped silicon is removed that greatly contribute to improve the electrical characteristics. Finally, the films were crystallized into the solid phase using a standard furnace annealing without breaking vacuum at 600°C for 8h. AFM measurements performed on silicon films show a low surface roughness around 2,4nm (RMS).

Photolithography and reactive ion etching were used to define the active island area. Doped poly-Si layer was first dry etched still the intrinsic polycrystalline film. A RCA clean and buffered HF dip establish clean interfaces between undoped channel layer and the following gate insulator. After the deposition of a 80-nm thick AP-CVD SiO₂ at 430°C as the gate oxide layer, a furnace-annealing of SiO₂ was carried out at 600°C in N₂ ambient during more than 1h to improve the properties of the oxide. Via were formed on oxide using conventional lithography and wet etching. Finally, 300-nm-thick chromium layer was put down using thermal evaporation and wet etched as contact electrodes. Here Cr is integrated to avoid an undesirable interaction (hillocks, cracks) between Al metallization and ITO-anode electrode during the wet etching of ITO for anode patterning. The pixel storage capacitor C_s is formed in the same time with the gate SiO₂ layer used here as dielectric between the chromium source-drain level and the underlying P+ (or N+) silicon layer. The present process does not include any hydrogen plasma treatment to ensure an optimal stability.

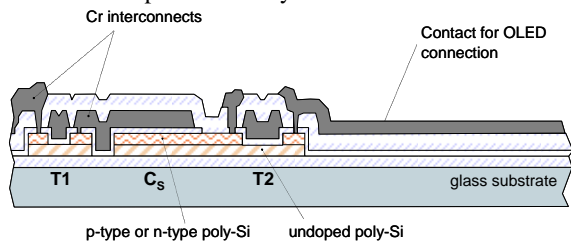


Figure 1. Cross-sectional diagram of an active pixel circuit illustrating the TFT architecture. Here the OLED is formed separately and connected to drive-TFT

Bottom-emitting OLED with a simple structure were realized on glass substrates. A 100-nm thick indium tin oxide (ITO) layer was deposited by sputtering and wet etched as the bottom-anode electrode. An O₂ plasma treatment is carried out before organic deposition in order to improve the ITO surface. Next all layers were deposited through a shadow mask by thermal evaporation in a vacuum system following previous report [7]. The organic stack consists on a p-type doped hole transport layer deposited on the ITO anode, an interlayer, the

emissive layer, a second interlayer and a n-type doped electron transport layer. Finally, a LiF/Al bi-layer was used as cathode electrode. The diode fabrication was finished by a glass encapsulation to ensure a high lifetime of devices.

The electrical characteristics of drive TFT and OLED were measured at room temperature using a standard semiconductor parameter analyzer (HP4155B) and a pulse generator unit (HP41501A).

Typical OLED characteristics

Green, red and blue emitting OLED devices have been fabricated. Figure 2. shows the current-luminance/voltage (I-L-V) characteristics of three R,G,B test OLED, each group separated by 8mm. Very low variations are measured between the 3 groups (<30mV at 500nA). Thus possible future pixel non-uniformity cannot attributed to the diodes but probably to TFT variations.

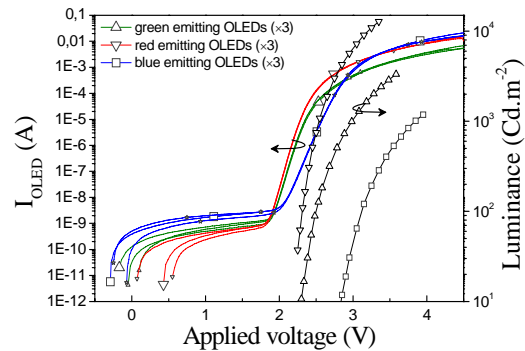


Figure 2. I-V and L-V characteristics of bottom-emitting test OLED measured in forward mode (area of 36,3mm²)

Electrical characteristics of SPC-TFT

The random distribution of grains boundaries in the polysilicon active layer often results in variations of both threshold voltage V_T and mobility μ. In order to evaluate the eventual predominance of one of these parameters many samples have been tested with different conditions. First TFTs are fabricated using silicon films deposited with disilane (p-type TFTs p-Si₂H₆) or silane (n-type n-SiH₄ or p-type p-SiH₄) as source gas. It is known the amorphous silicon films deposited with disilane and then solid-phase crystallized have larger grains [reference]. Typical values and deviations of threshold V_T, ON/OFF current ratio, sub-threshold slope (S) and field effect mobility in saturation (μ_{SAT}) are summarized in Table 1. Obviously, Si₂H₆ TFTs exhibit higher performance.

Table 1. Electrical parameters for p-type and n-type TFT (x20) fabricated using polysilicon films deposited with silane or disilane as source gas

W/L=40/20	V _T (V)	I _{ON/OFF}	S (V.dec ⁻¹)	μ _{SAT} (cm ² .V ⁻¹ .s ⁻¹)
p-SiH₄	-11±0,5	>10 ⁶	1,2	39±8
p-Si₂H₆	-9 ±0,8	~5.10 ⁶	0,8	54±13
n-SiH₄	7 ±0,6	>10 ⁶	1,1	91±17

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Figure 3. shows transfer characteristics of poly-Si TFT (obtained from silane gas) when the drain voltage equals 1V, 5V and 10V.

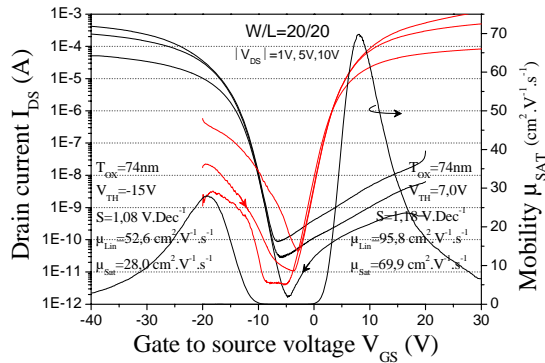


Figure 3. Transfer characteristics of non-hydrogenated p and n-type polysilicon TFTs fabricated using furnace-annealed polysilicon and without LDD structure.

The field effect mobility in the saturation regime μ_{sat} was calculated at $V_{DS}=\pm 5V$ from eq.(1) which is independent of V_T parameter.

$$\left(\frac{\partial \sqrt{I_{Dsat}}}{\partial V_{GS}} \right)^{-2} = \frac{2L}{W} \times \frac{1}{\mu_{sat} C_{OX}} \quad (1)$$

where C_{ox} is the capacitance per unit area of the gate oxide ($\sim 46nF.cm^{-2}$) and L/W is the channel length/width ratio.

From our experiments, the variation of the mobility parameter μ_{SAT} is often higher than the fluctuation of threshold V_T parameter. Figure 4 presents the $\partial gm_{sat}/\partial V_G$ (where gm_{sat} is the transconductance in the saturation region) of p-type and n-type channel TFTs with $W/L=40\mu m/20\mu m$. Measurements are carried out on arbitrary locations within the area of $2 \times 2cm^2$ at $V_{DS}=\pm 5V$. This representation is useful to determine the threshold voltage which corresponds to the hump of the curve. As a better precision is expected, it is here preferred to conventional linearly extrapolation. The resulting variation of threshold voltage is about 5% for p-channel and 10% for n-channel. Higher variations of gm_{sat} are measured (17% and 14%). Finally drain current change seems to be highly related with mobility variations. This phenomenon can be also evaluated from OLED pixel circuits.

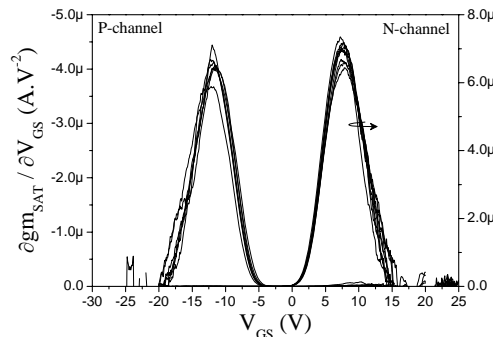


Figure 4. Electrical performances of n and p-channel TFT measured over a $2 \times 2cm^2$ area.

Evaluation of uniformity using AMOLED pixel circuits

The characteristics of SPC-poly-Si-TFT are relatively uniform. Then simple 2-TFT and one capacitor pixel structure, Fig. 5a, can be used. However in order to shrink V_T fluctuations, a compensation circuit was also implemented close to each 2-TFT circuits. The circuit reported by Jung *et al.* [9] was designed for p-type and n-type TFT (Fig. 5b). It can alleviate the non-uniformity issue using a diode-connected TFT for V_T variation-compensation. The merit of this voltage-programmed circuit is mainly its simplicity (addressing signals, no additional line).

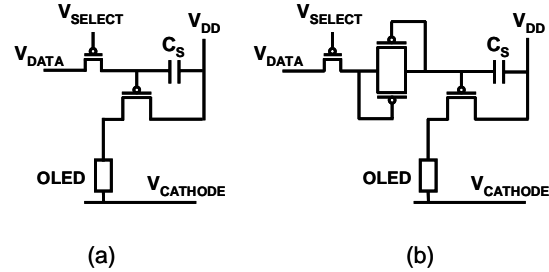


Figure 5. Circuit diagrams of p-type pixel circuits using (a) a simple configuration (b) a threshold compensation [9].

The width to length of the switch and drive TFT are $10\mu m/10\mu m$ and $40\mu m/10\mu m$ respectively. Our design requires a drive TFT W/L ratio of 4 so that low input voltage can be applied despite our high V_T .

The human eye is not as sensitive to the long-range non-uniformity of brightness as to short-range disorder. So current dispersion have been here preferably evaluated on local areas. Figure 6. shows the distribution of the current flowing through the OLED as a function of the power voltage V_{DD} (or $V_{CATHODE}$) for p-type and n-type TFTs. Voltages are applied over a wide range indicating that the short channel perturbation occurred only for voltages higher than 10V. The non-uniformity of driving current (defined as the maximum difference of currents divided by the average) of p-type circuits is obviously lower than that of n-type (22% and 36% respectively at $\sim 0.5\mu A$).

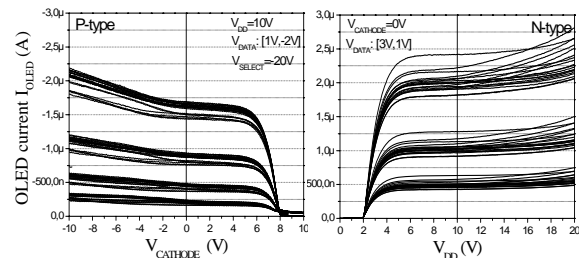


Figure 6. Drive current measured in DC mode for p-type and n-type 2-TFT pixel circuits ($W/L=40/10$).

Note that due to the high efficiency of this blue emitting OLED, the quadratic behaviour of current is not

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apparent. Then, drive current rises quickly at OLED threshold voltage ($\sim 2V$).

To investigate more the origin of current fluctuations, p-type circuits have been operated in pulsed mode. Figure 7. shows the controlled voltage on gate node of drive-TFT in case of a pixel circuit with compensating cell. The threshold compensation is effective and the leakage currents through the TFT are low enough to sufficiently maintain the charge in the storage capacitor during one frame period. Nevertheless high voltages are required due to the high threshold value and a large timing delay is required for a full compensation ($\sim 1ms$).

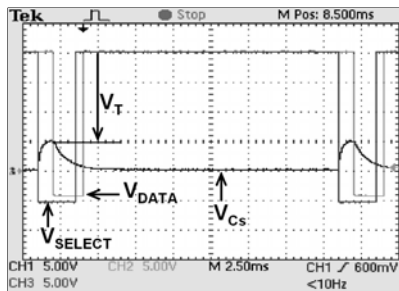


Figure 7. Transient measurements during threshold voltage evaluation using p-type 4-TFT pixel circuit.

Figure 8. shows the measured transient waveforms of the OLED current I_{OLED} of conventional 2-TFT pixels and threshold-compensated 4-TFT circuits along one column. From these results the contribution of the compensation cell on the non-uniformity is about 10%. Here again the influence of μ_{SAT} is significant.

After pulsed operations, transfer characteristics of these drive-TFT were performed. Extracted threshold V_T and

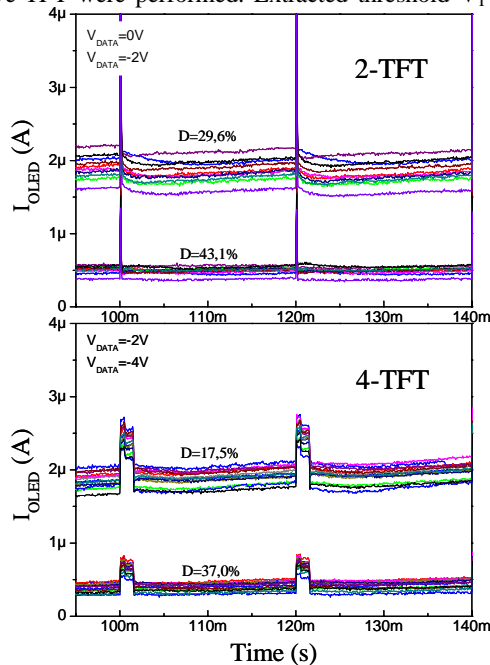


Figure 8. Transient waveforms of current flowing through an OLED. Measurements are carried out from several circuits in case of (a) 2-TFT and (b) 4-TFT pixels.

mobility μ_{SAT} revealed similar values than those previously mentioned.

Conclusion

In this paper, the current variations of p-channel and n-channel drive TFT fabricated from furnace-annealed polysilicon films have been investigated on active OLED pixels. In investigated local areas, results show that the driving current is mainly affected by random variations of the field effect mobility ($>10\%$). A threshold-compensation has been also implemented in circuits. Its effect is not really efficient to solve non-uniformity of driving current. This suggests that driving active pixel circuits using TFT with short dimensions and high performances is a real challenge and requires a technique for mobility compensation. Nevertheless SPC using furnace annealing has great potential for fabricating excellent TFT's on large-area glass substrate and in batches. Thus it is an attractive method to process AMOLED backplane.

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