A Study on the Improvement of Address Discharge Time Lag in AC PDP at Low Temperature

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Abstract: *The plasma display panel is the image expression display using gas discharge plasma. However gas discharge characteristics vary with temperature as gas discharge is sensitive to temperature. Particularly, the discharge time lag extends a lot in low temperature and it is known as the cause which hinders high speed addressing which is essential for the size enlargement of the panel. Accordingly this research aims at identifying the temperature-dependent discharge characteristic. The lower temperature gets, the longer addressing discharge time lag becomes. Particularly the statistical time lag extends much in low temperature. Sufficient heightening of electric field effect shortens discharge time lag in low temperature. Also, when priming particles are sufficiently supplied, stable discharge can be performed regardless of the influence of temperature.*

Keywords: PDP, Address Discharge Time Lag, Priming Particle

Introduction

Modern Society is becoming 'information society' swiftly and the information quantity is increasing rapidly in the aspect of information transfer volume. And the role of the display device through which humans can contact with information easily is becoming more important as time passes. Currently researches on a new display device which can replace the Cathode Ray Tube (CRT) which is most widely used among display kinds is going on actively due to the limited possibility of improvement through CRT for size enlarging, weight lightening, and surface flattening.

The plasma display panel(PDP), one of the next generation display device kinds which can be used covering the range of TV, computers and the internet realm in the digital age of 21st century, is one which expresses letters and graphics using plasma made by gas discharge. PDP draws the attention as the next generation display device as it has many advantages such as the availability of size enlargement in larger than 60 inch, high resolution, wide viewing angle, long longevity and light weight.[1]

In the current ADS (Address and Display period Separated) mode which is opted mostly for plasma display operation, the brightness decreases as sustain period is shortened because of long address period. Accordingly screen quality improvement will be available through the enhancement of brightness and the reduction of dynamic false contour noise by shortening the time allocated to address field and adding this shortened time to sustain period. To shorten address period it is necessary to reduce address discharge time lag. However, there is the problem that misfiring happens in low temperature due to the rapid extension of address discharge time lag. Nevertheless, researches on this problem are almost none currently.

This research identified the phenomenon that the discharge time lag of PDP extends in low temperature through experiments and compared between the results from the case that address voltage is raised and the case that priming particles are supplied for shortening discharge time lag.

Experimental

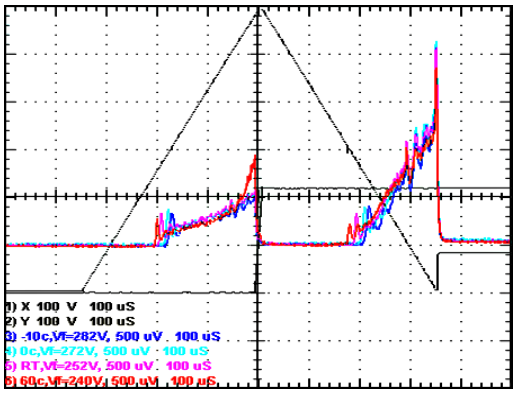
In the experiments a test panel of 7.5 inch XGA level (Ne+10%Xe) is used. A pulse generator (HVA800, FT lab), a digital oscilloscope (TDS3054B, Tektronix), a cooling device (Acetec), and a photo detector (C6386-01,Hamamatsu) as a light waveform measurer are used for the experiment processing.

In this study the measurement of discharge time lag is conducted by measuring the generated output light during address discharge by photo detector instead of measuring discharge current.

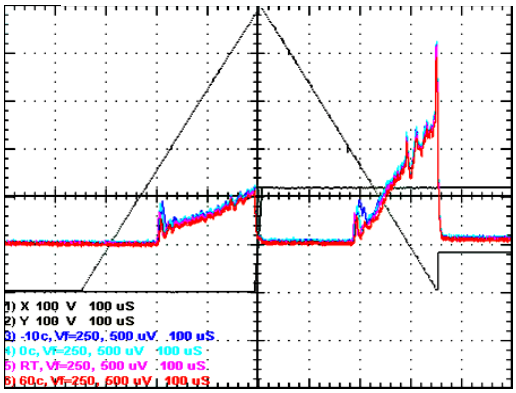
Results and Discussion

Figure 1 shows the variation of light waveform in reset period in the case of partial temperature control and in the case of whole temperature control, respectively. In the case of partial temperature control a firing voltage changes with temperature. The firing voltages in -10 ^{o}C and in 60 ^{o}C show the difference of more than 40 V. The cause of image sticking problem has been thought to be a firing voltage variation due to temperature variation simply. That is, the temperature variation on a part of a panel changes the gas density of that part. When the temperature on a part of a panel rises the gas density of that part falls and the mean free path of electrons is lengthened. Accordingly electrons can obtain more energy by the electric field of same strength and the firing voltage decreases.[2]

Figure 1(b) illustrates the firing voltage variation in reset period in the case of temperature variation on a whole panel. In this case firing voltage does not change as gas density is equal on the whole panel because the panel is closed up by itself. Figure 2 shows address discharge light waveform corresponding to a temperature variation. An address voltage of 70 V is applied in the address discharge. It is identified that the lower temperature falls, the weaker the light waveform gets and the longer the discharge time lag becomes, both in partial temperature variation and in whole temperature variation.



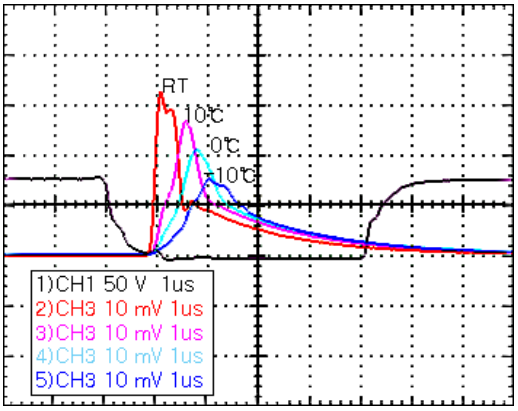
(a) Partial Temperature Control



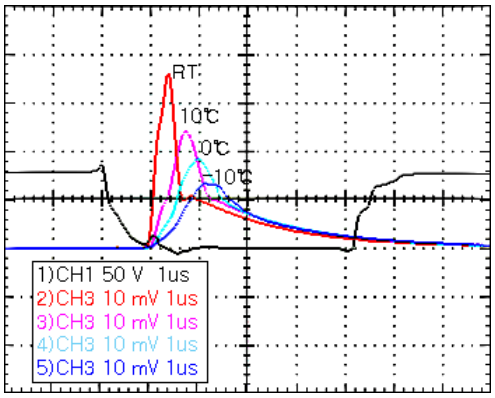
(b) Whole Temperature Control

Figure 1: Light Waveforms in reset period vs. Temperature

Though the firing voltage does not change in the case of whole temperature variation, the discharge light waveform in whole temperature variation shows the tendency which is similar to in partial temperature variation.



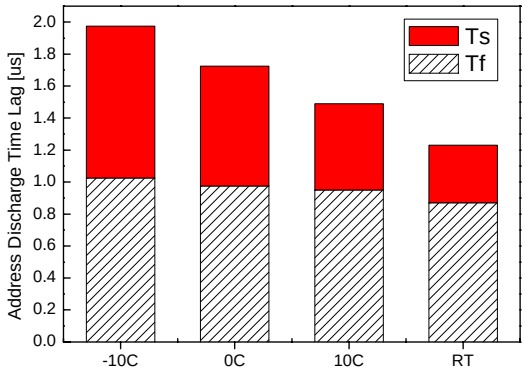
(b) Whole Temperature Control



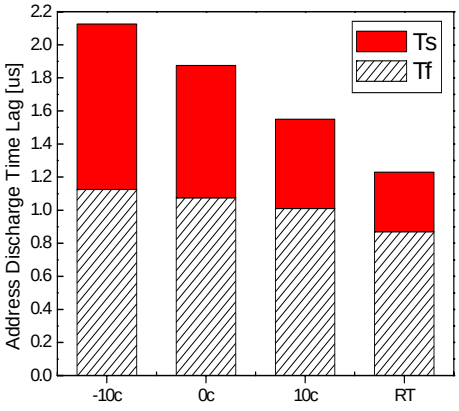
(b) Whole Temperature Control

Figure 2: Light Waveforms in Address Period vs. Temperature

Figure 3 shows the variation of discharge time lag corresponding to temperature variation. In the figure it is found that as panel temperature decreases lower, discharge time lag increases more and statistical time lag increases a lot particularly. The discharge time lag extends almost



(a) In Partial Temperature Control



(b) In Whole Temperature Control

Figure 3: Address Discharge Time Lag vs. Temperature

above 2 times in -10°C compared to the lag in room temperature. Address misfiring in low temperature, which becomes a big hindrance for high speed addressing, can occur because of this phenomenon.

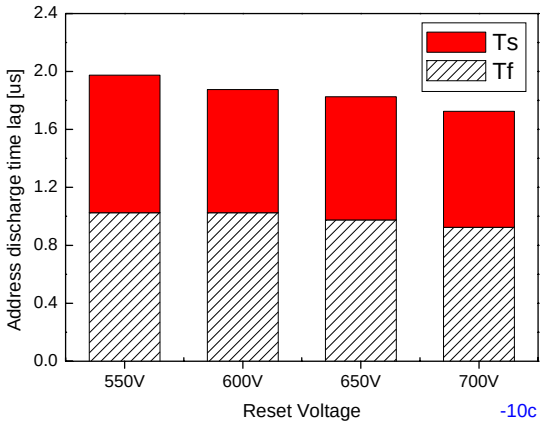


Figure 4. Address Discharge Time Lag vs. Reset Voltage(-10°C).

Figure 4 shows the variation of address discharge time lag corresponding to reset voltage variation in -10 °C. In the figure it is found that address time lag is being

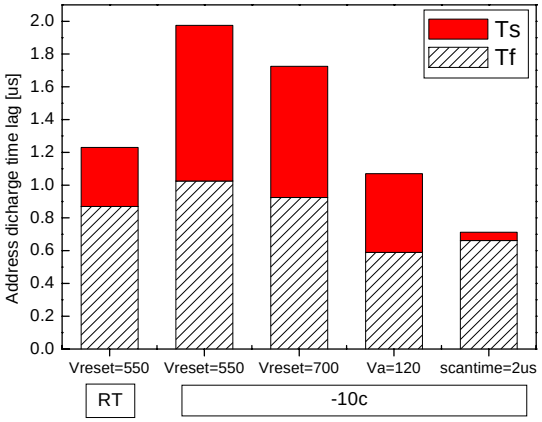


Figure 5. Address Discharge Time Lag with Reset Voltage, Address Voltage, Supplying Priming Particles, and Temperature.

Figure 5 is the result of the comparison between the case that reset voltage and address voltage is raised each and the case that sufficient priming particles are supplied, in order to improve the increased discharge time lag in -10 °C. Discharge time lag extends to 2 μs from some 1.2 μs when temperature falls to -10°C from room temperature. Discharge time lag is shortened to 1.75μs when reset voltage is raised to 700 V from 550 V in -10°C. Discharge time lag, which is similar level to the case in room temperature, is obtained when address voltage of 120 V, which is the maximum limit, is applied. In the early time of address period a large quantity of priming particles which are made in reset period are supplied to the discharge space. At 2μs passing point when sufficient priming particles are supplied in low temperature, much shortened address discharge time lag and stable discharge processing are found.

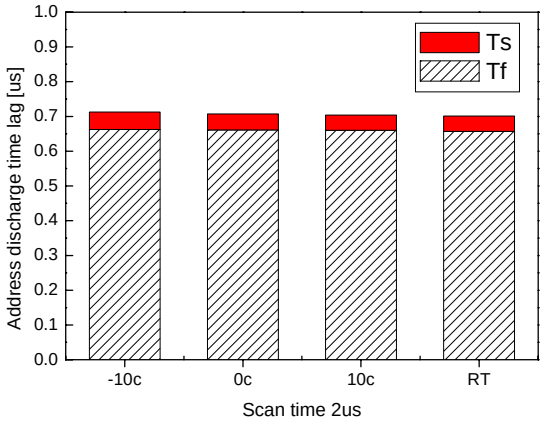
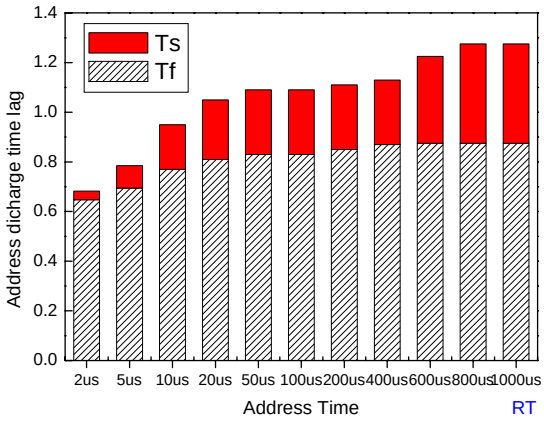
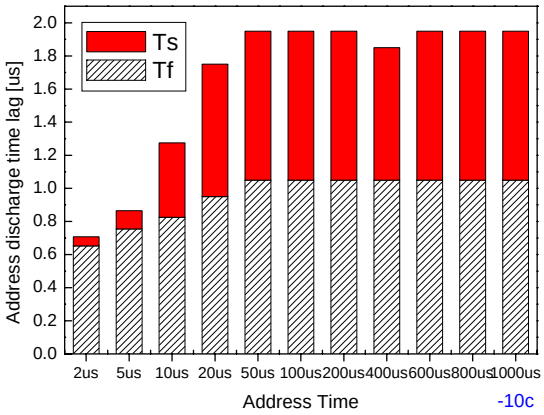


Figure 6. Address Discharge Time Lag vs. Temperatures (scan time=2us).



(a) Address Discharge Time Lag vs Address Time (Room Temperature)



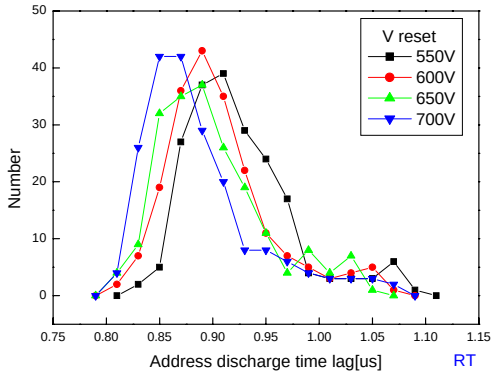
(b) Address Discharge Time Lag vs. Address Time (-10°C)

Figure 7. Address Discharge Time Lag vs. Address Time

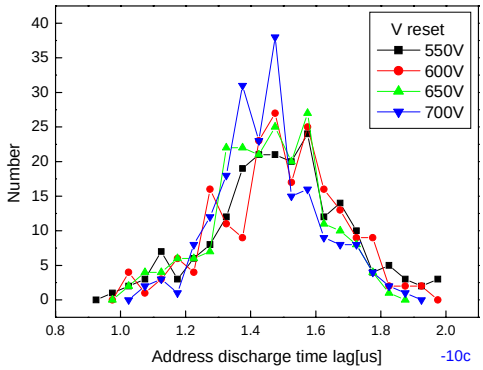
Figure 6 shows the result of discharge time lag measured at 2 μs passing point when sufficient priming particles are supplied, as a function of temperature. The noticeable fact in the result is that the variation of

discharge time lag is almost not influenced by temperature variation if priming particles are sufficiently supplied.[3]

Figure 7 shows address discharge time lags in address period. In this period address time lag extends longer increasingly in accordance with time passing because the number of priming particles, which were made in reset period, decreases. In room temperature priming particles made in reset period influence up to the point of 800μs from the beginning of address period and discharge time lag is extended longer gradually from the beginning of address period to this point. However, in -10 ^{o}C priming particles influence only within the point of 50μs, and afterwards it does not influence on discharge time lag.



(a) Room Temperatue



(b) -10^{o}C

Figure 8. Distribution of Address Discharge Time Lag vs Reset Voltages on Address Time of 1000 μs.

Figure 8 shows the distribution of discharge time lags with reset voltages on the point of 1000μs passing in address period. In room temperature the center of distribution is moved to the left to some extent by the influence of prime particles. However, in -10^{o}C priming particles almost cannot exert influence. The possibility that the life time of priming particles is shortened in low temperature and exert influence on address discharge is presumable.

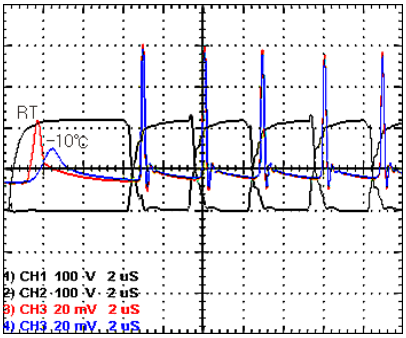


Figure 9. Light Waveforms by Temperatures in Sustain period

Figure 9 shows the discharge light waveform in sustain period. In the figure it is found that the first sustain discharge shows the similar tendency with address discharge as a function of temperature. The discharge light waveform of the second time and afterwards show the same shapes regardless of temperature. This is consistent with the address discharge waveform when priming particles are sufficiently supplied.

Conclusion

High speed addressing makes it possible to design PDP in better quality as it reduces address period. However, in low temperature address misfiring can cause screen quality degradation as address discharge time lag is increased rapidly. The reason for that address discharge time lag is extended longer in lower temperature is not yet revealed. In this research the phenomenon that discharge time lag of PDP is increased in low temperature is identified through experiments and the comparison between the results of reset voltage raising, address voltage raising, and sufficient priming particles supplying for shortening discharge time lag is conducted. Discharge time lag which is rapidly increased in low temperature is reduced very effectively when sufficient priming particles are supplied. Particularly statistical time lag is reduced a lot, which makes stable addressing available.

References

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