A New Reset Waveform with Negative Ramp Pulse in ac PDP

Hyerim Choi, Myunghwan Oh, Jungwon Kang
Department of Electronics and Computer Engineering, Display device laboratory
Dankook University
Hannam-ro Yongsan-gu, Seoul, Korea, 140-714
zenca1997@gmail.com

Abstract: *Conventional reset waveform applied to the commercial PDP uses a positive ramp pulse. This paper proposes a new reset waveform with negative ramp pulse. The reset waveforms, especially focused on ramp area, were examined with 2 dimensional fluid simulation code. The proposed negative reset waveform showed much lower ignition voltage (~70V) as compared with the conventional reset waveform. When the positive ramp pulse was applied, the positive-charged ions drifted toward the sustain and address electrodes. However, when the negative ramp pulse was applied, all of the positive-charged ions are collected on the scan electrode. It is found that the ignition voltage of reset discharge due to the negative ramp pulse was lower than that of positive ramp discharge.*

Keywords: PDP; reset period; negative ramp reset.

Introduction

Digital broadcasting and high quality contents are leading the new market of the flat panel displays. A plasma display panel (hereinafter "PDP") is the one of promising display having large size, full color and wall mountable characteristics [1-2]. The driving method of the address and display separated (ADS) scheme has been used principally in PDP [3-4]. This scheme is consisted of three periods; reset, address and sustain.

From the beginning of HDTV broadcasting, the demand of high resolution display having more than 768 scan-lines is increased compared to the demand of common display with 468 scan-lines. As the resolution is increased, the required time of the address period is increased and the pixel pitch is decreased when the displayed area is fixed. Because of the increasing time in address period, the allocated time for the reset and sustain periods is decreased. If the pixel pitch is decreased, the discharge volume in a unit cell is decreased. These caused the problems such as low luminance, address instability and increment of driving voltage [5]. To improve the characteristics of PDP, it is necessary to find a new reset waveform having lower voltage and shorter time than those of conventional waveform. In this paper, a new reset waveform having negative ramp pulse is proposed to achieve this purpose.

Results

In the ADS scheme, the reset pulse is applied to the scan electrode. The role of applying the reset pulse is to provide enough seed electrons in the cell and to equalize the wall charge on electrodes for subsequent successful sustaining discharge. In this paper, the reset waveform, especially focused on ramp area, was simulated by using of 2 dimensional fluid code [6].

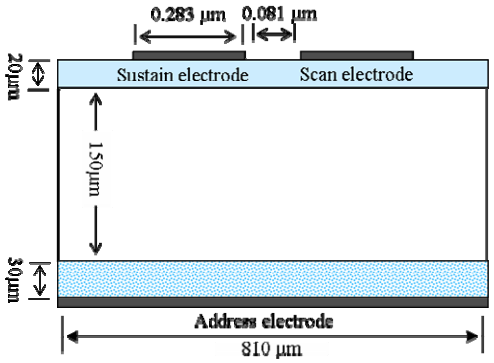


Figure 1. Geometry of calculated PDP cell

The discharge gas of Xe10%-Ne at 500 torr was selected. The thickness and relative dielectric constant of the front dielectric layer were 20 um and 10 respectively, and those of the rear dielectric layer were 30 um and 5. The secondary electron emission coefficient (= γ) of Ne and Xe gases are 0.8 and 0.05 respectively.

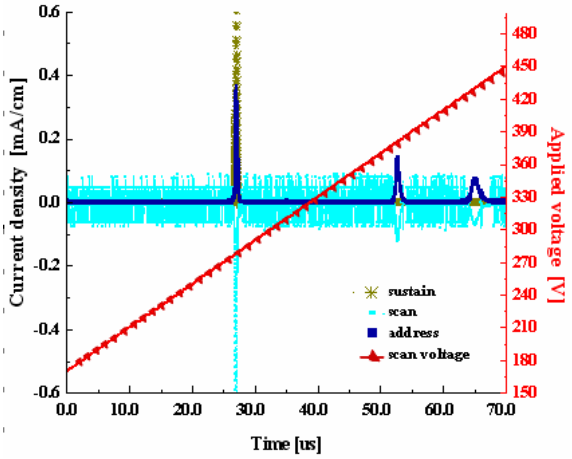


Figure 2. Conventional positive ramp pulse and current peaks from three electrodes during positive ramp-up

Figure 2 shows the conventional reset waveform having positive ramp pulse. During 70 us, the ramp reset pulse was increased form 170 V up to 450 V. The increment of voltage was set to 4 V/us. The first reset discharge was ignited at 280 V after 28 us was passed from the beginning. Weak discharge occurred between scan-sustain and scan-address electrodes. The positive wall

charges were accumulated on the sustain and address electrodes during positive ramp-reset period and the negative wall charges were accumulated on the scan electrode. Therefore the negative current peaks from the scan electrode and the positive current peaks from sustain and address electrodes were observed.

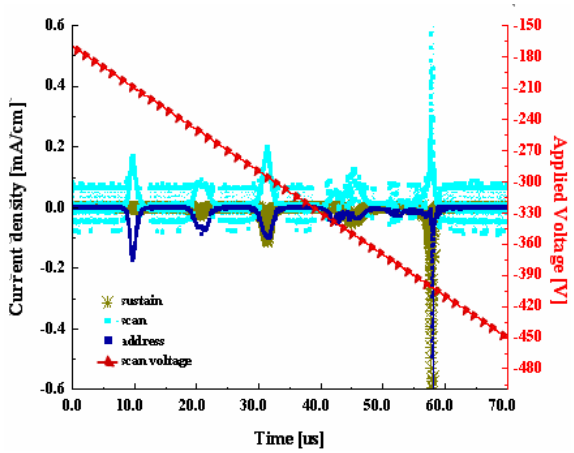
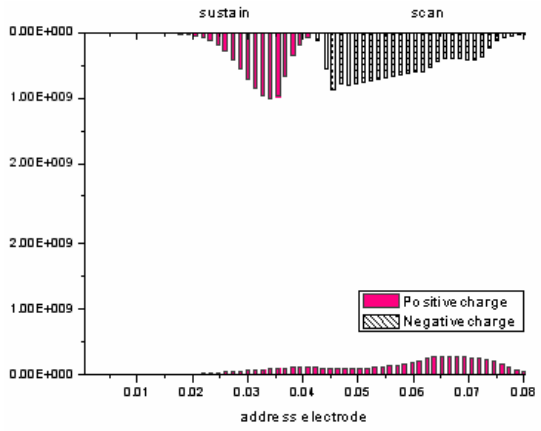
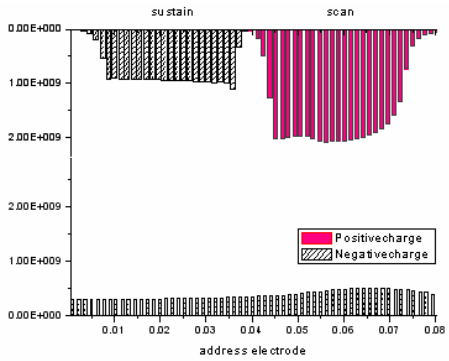


Figure 3. Proposed negative ramp pulse and current peaks from three electrodes during negative ramp-down

Figure 3 shows the proposed reset waveform having negative ramp pulse. During 70 us, the ramp reset pulse was decreased form -170 V up to -450 V. The decrement of voltage was set to -4 V/us. The first reset discharge was ignited at -210 V after 10 us was passed. The absolute amplitude of ramp voltage and consumed time were lower and shorter than those of positive ramp pulse. When the positive ramp pulse was applied, the positive-charged ions drifted toward the sustain and address electrodes. However, when the negative ramp pulse was applied, the positive-charged ions are collected on the scan electrode. Therefore the ignition voltage of reset discharge due to the negative ramp pulse was lower than that of positive ramp discharge.



(a)



(b)

Figure 4. Wall charge profile at 70 μs
(a) Conventional positive ramp reset pulse
(b) Proposed negative ramp reset pulse

Figure 4 shows accumulated wall charges on electrodes at 70 us. The case of negative reset pulse is founded much more accumulated wall charge (~50 %) than the case of positive reset pulse. When it compares positive reset pulse with negative reset pulse, negative reset pulse has the advantageous results that can be lower ignition voltage and generate sufficient wall charges.

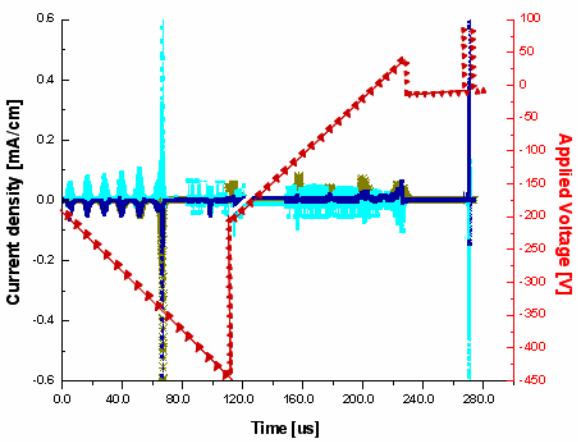


Figure 5. Full reset waveform with negative ramp pulse and current peaks from three electrodes

Figure 5 shows the full-reset waveform having the proposed negative ramp pulse. First ramp pulse for accumulating wall charge on electrode is negative ramp-down pulse and it is applied to scan electrode from -190 V up to -450 V during 107 μs. Second ramp pulse for clearing wall charge on electrode is positive ramp-up pulse and it is applied to scan electrode from -190 V up to 50 V during 110 μs. Weak discharge occurred between scan-sustain and scan-address electrodes and the wall charges is accumulated sufficiently and redistributed on electrode as it is showed in Figure 6. Through address pulse applied, wall charges accumulated on electrodes and it is possible to operating the sustain function consecutively in next period. New reset waveform is also executed the part as conventional driving waveform in ac PDP.

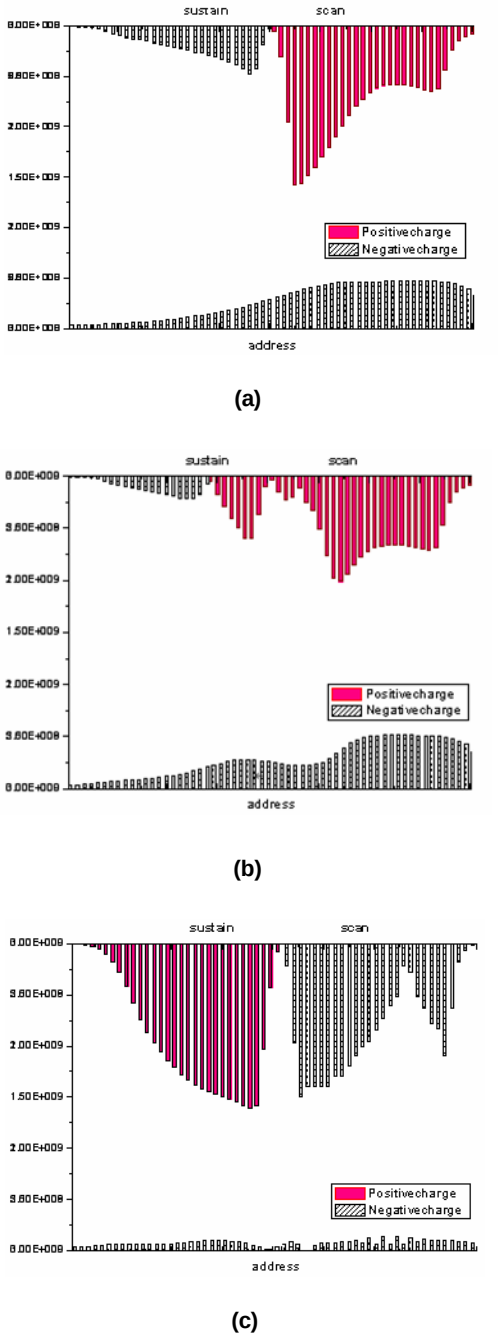


Figure 6. Full reset waveform with negative ramp pulse and wall charge with time
(a) 1st slope for generating wall charge in reset period
(b) 2nd slope for clearance wall charge in reset period
(c) wall charge profile after address pulse applied

Impact

Our studies improved driving character such as operating voltage and consumed time of a high resolution in ac PDP.

References

1. S.Mikoshiba, Inform.Display, Vol.10, pp.21-23, 1994 *Process Safety Progress*, Vol. 13, No. 4, pp. 227-233, 1994.
2. J.P.Boeuf, V.Punset, A.Hirech and H.Doyeux, *J.Phys*.Ⅳ France 7, 1997
3. J.P.Boeuf, *Journal of Physics D: Applied Physics*, 2003
4. Yoshikawa K, Kanazawa Y, Wakitani W, shinoda T and Ohtsuka A 1992 Japan. *Display* 1992
5. Jungwon Kang, *IEEE Trans. Electron Devices*, Vol.52, No.5, pp.922, 2005
6. C.Punset, S.Cany, and J.P.Boeuf, *Journal of Physics*, Vol.86, No.1, pp.124-133, 1999