Electrical characterization of solution processed MEHPPV/CNPPV hetrostructures.

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Abstract: *Hetrostructured light emitting diodes are one of the promising candidates for flat panel display and lighting applications. Fabrication of hetrostructure devices using solution processing of light emitting polymers has been a challenge due to interface intermixing between two layers. The quality of the space charge distribution in the device is due to different Fermi levels of the two polymers hence the polymer/polymer interfacial space charge plays an important role in determining device characteristics.*
In this paper, a strategy has been developed to grow hetrostructures and evaluate of intermixing at the interface during solution processing. We investigate the ac electrical response of double layered polymer electroluminescence devices using the MEHPPV and CNPPV as the model polymers for hetrostructure formation by conventional spin casting methods. Frequency dependence impedance spectroscopy studies have been done in the range of 100Hz to 1MHz. We show that it is possible to infer the relative degree of inter- mixing from electrical characteristics.

Keywords: *PLEDs; blending; charge accumulation at interface.*

Introduction

The promise of low cost, high efficiency display with wide viewing angle makes organic and polymer light emitting diodes potential candidates for replacement of existing space technology such as liquid crystal and plasma[1]. In contrast to vacuum evaporation techniques needed for small molecules based OLEDs, the solution processibility of polymers holds the possibility of large area applications. The conventional spin coating of multiple layers is the most cost effective way of fabricating PLEDs on large area substrates. However, often the layers need be spin cast from solution which is common to the different layers. This result in intermixing of the layers during processing and hence desired interface cannot be obtained. This is a key problem for spin casting of hetrostructures. On the other hand, it is also known that a controlled level of intermixing between ETL and HTL improves device quality. It appears that if strategies are developed to enable spin casting of multiple layers and evaluating the effect on the degree of intermixing of the two layers, it is possible to fabricate such devices under controlled conditions. PLEDs are

basically solution processed, fabrication of multilayer PLEDs is difficult. The problems associated with casting different layers using the same solvent include morphological changes of the first layer, dissolution of the top few nano-meter of the first layer and possibility of blending of two polymers. It is well known that the processes leading to luminescence and the charge transfer leading to solar cell effect are influenced by polymer-polymer interface and surface morphology [2]. The morphology of layer and quality of polymer-polymer interface play an important role in tailoring the device characteristics such as low operating voltage and high luminescence.

In this paper, we investigate different methods of spin-casting of MEHPPV and CNPPV to form PLEDs principally to asses the degree of intermixing at the interface and its impact on electrical characteristics of the diodes. Impedance spectroscopy has been a powerful tool to study such interfaces [3-7]. We extend its use to evaluate the impact of intermixing as electrical properties of spin cast hetrostructures formed by depositing CN-PPV and MEH-PPV. We show that it is possible to infer effective thickness of these layers from such studies.

Experimental Details

ITO coated glass substrates were patterned using standard lithography technique. Ozonization was done for 10 minutes to enhance the work function of ITO. PEDOT: PSS was spin coated at 1500rpm followed by vacuum drying at 130^{o}C for an hour. Commercial MEH-PPV (Aldrich) and home made CN-PPV were dissolved in similar organic solvents at different concentrations (6mg/ml and 8mg/ml respectively) and stirred on magnetic stirrer for twelve hours. The solutions were filtered thoroughly. MEH-PPV solution was spin coated on ITO under nitrogen atmosphere for 100nm thickness and then vacuum dried at 130^{o}C for an hour. We have varied the extent of coverage of CNPPV prior to its spin coating by three different methods: (A) the MEH-PPV layer was removed to create a valley over a sufficient area (1.5×5cm^2), in the middle of the substrate, and then the CN-PPV solution was spread gently in the valley and then spin coated; (B) the CN-PPV solution was spread in the middle of the MEH-PPV layer and then spin coated; (C) the CN-PPV solution was spread over the whole layer of MEH-PPV and then spin coated. We will compare the characteristics of the three types of devices in the rest pf the paper. The MEH-PPV layer is coated as in conventional processing all over the substrate on the PEDOT: PSS layer. All the substrates were vacuum dried at 130^{o}C for an hour. Finally, 1000 Å thick

aluminum cathode was vacuum evaporated at the rate of 1Å/sec.

The thickness measurements were performed using Alpha-Step profilometer (Tencore alpha-Step 500 Profiler). The I-V measurements were done using Keithley 4200 semiconductor parameter analyzer and the impedance spectroscopy was carried out using Agilent 4294 A impedance analyzer. The frequency dependent impedance data has been obtained by superposing an ac signal of 20mV for different dc bias.

Results and Discussion

The devices have been named according to the mode of spin coating of the CN-PPV layer on MEH-PPV layer, with the CN-PPV solution being dispensed (a) to a central valley from where MEH-PPV have been removed, (b) at the middle of the MEH-PPV layer and (c) spread all over the MEH-PPV layer prior to spinning. The resultant devices are referred to as devices A, B, C respectively as explained in the last section. We expect largest degree of mixing of the two layers to occur in the case of C, while the smallest in case of A.

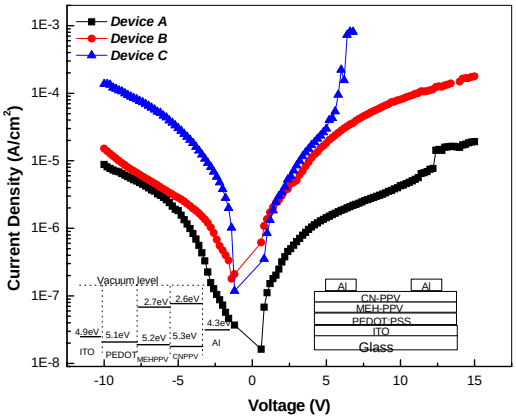
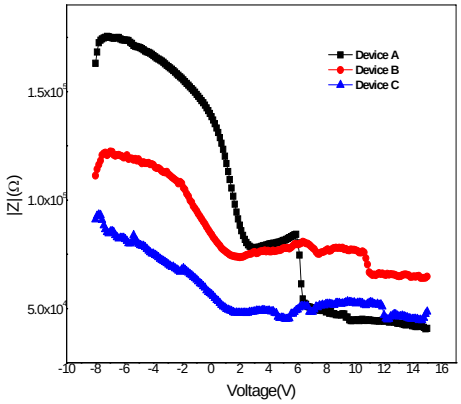
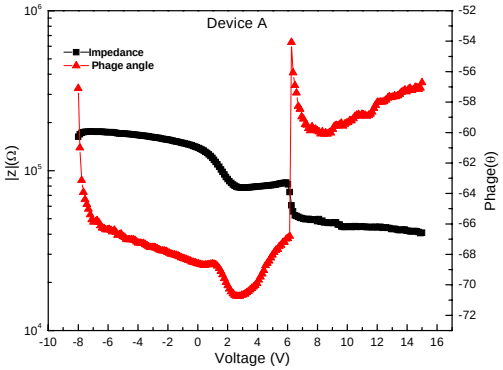


Figure 1. I-V characteristics of the devices A, B &C

Fig.1 shows a comparison of I-V curves of the three devices. Clearly the device C is the most leaky in reverse bias and shows a large jump at about 5V in forward bias corresponding to a trap filled limit voltage. The intermixing of the two layers in the green state seems to produce a large concentration defect states leading to this jump in forward bias current. In contrast, the device A, where we expect least mixing, does show existence of resistive bilayer in the structure.The I-V characteristics of sample B, where mixing is expected to be moderate, shows I-V curves typically expected of a heterostructure PLED, with leakage current being intermediate to the case of other two samples. The turn-on voltage is approximately similar in all the three cases and lies in the range of 2.8-3.0 V.



(a)



(b)

Figure 2. (a) Voltage dependence of impedance for all three devices (b) Impedance and phage angle for device A

We further investigate the voltage dependence of impedance of the three devices as shown in Fig.2 (a). Clearly, device A has the largest impedance in reverse bias in conformity with steady state I-V characteristics. The turn-on voltage for forward injection is also graded being high and sharp for the case of sample A. For this device, Fig.2 (b) shows the voltage dependence of the modulus of impedance | Z | along with phase angle variation, which clearly shows the transitions to various regimes of operation of the devices as voltage is swept from reverse to forward bias.

At large reverse bias, the samples behave as leaky capacitors with high impedance and phase angle in the range of 65° -70°. The turn-on is seen at 2.8-3.0 V and the injected current leads to minima in the phase angle. The step transition observed in both | Z | and C_p at 6V, clearly is due to accumulation of charge carriers at an internal interface of the device. This motivates us to monitor charge accumulation process through voltage dependence of capacitance in order to infer the degree of intermixing taking place in the three devices.

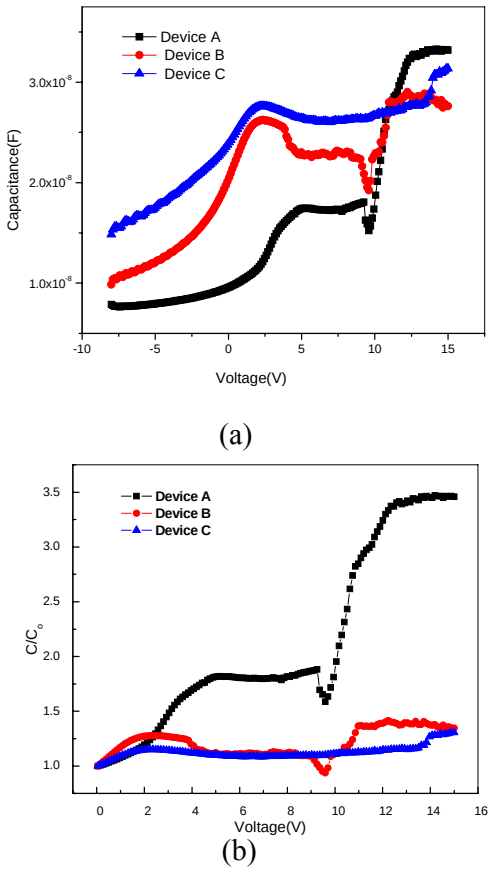


Figure 3. (a) Forward bias capacitance at 100Hz as a function of voltage, (b) normalized to respective zero bias capacitances for the three devices

Fig.3 shows the comparison of forward bias capacitance at 100Hz as a function of voltage both in their absolute values (Fig.3a), and as normalized to zero bias capacitances (Fig.3b). The voltage dependent capacitance has similar features in all three cases, the zero bias capacitance reflecting the variation of thickness for the entire stack in the sample. The occurrence of nearly constant plateau regions in the C-V curve indicates that these are controlled by the sub-structure geometrical capacitances. Beyond the onset voltage, the plateau can be attributed to the effective thickness across the interface at which accumulation occurs and the electrode. From independent measurements of thickness of the layers from the regions where no contact of the two layers is there, we know the thickness of the MEH-PPV and CN-PPV layers to be approximately 750Å each. The first transition beyond onset voltage gives the ratio of the total thickness to the effective thickness and which is 1.8, 1.2 and 1.1 for the samples A, B and C respectively. As the voltage is further increased there is a further step transition at 10, 12 and 14 V respectively for the three cases. This clearly indicates that the samples can be modeled as three layers in which a blended layer is sandwiched between the two pure layers of MEH-PPV and CN-PPV. The charge accumulation shifts from MEH-PPV-blend interface to the blend-CN-PPV interface. Hence the thickness of the blended layer at the interface can be inferred.

We also note that there are noticeable dips prior to the constant value plateaus in Fig.3. This shows that certain amount of defect charges at the interface need to be overcome before charge accumulation can set in at that interface. We also note that the turn-on voltage for the low voltage accumulation event is lower for the cases of layer thickness of the blend, whereas opposite is true for the high voltage accumulation event.

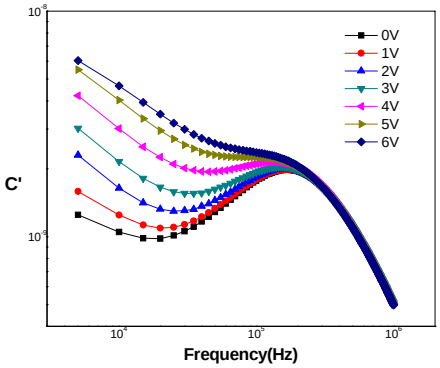
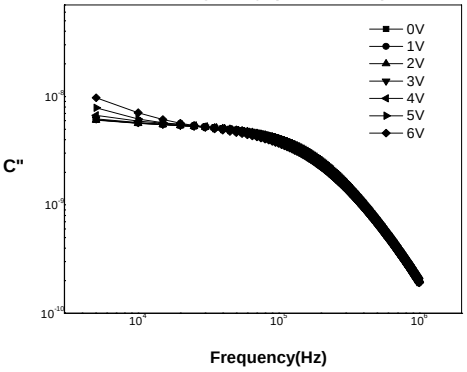


Figure 4. Real and imaginary part of capacitances



for the sample A for different voltages.

Fig.4 shows the frequency variation of real and imaginary part of capacitance for the sample A for different voltages. The low frequency regime shows significant variation with voltage, and hence the above analysis seems to be controlled by defect charge[8]. The forgoing analysis clearly needs to bee carried out in the low frequency regime. Fig.5 shows some typical Cole-Cole plot for the same sample for different voltages. Two large semi-circles, whose radii depend on voltage, can be inferred[9]. Typically, a series resistance and two RC parallel circuits in series are adequate to explain the Cole-Cole plots[10]. A detailed analysis is required to extract influence of the blended layer on such plots.

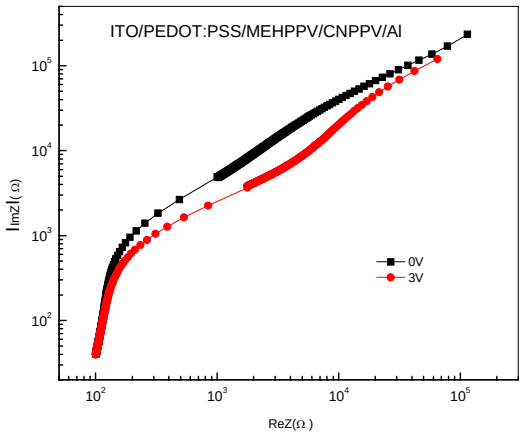


Figure 5. The Cole-Cole plot at two bias voltages for comparison.

Conclusions

We have explored three different methods of spin coating of CN-PPV on MEH-PPV in order to evaluate the extent of intermixing due to common solvent. The intermixing gives rise to a blended layer and its extent is estimated on the basis of impedance studies specifically voltage dependent capacitance. The method can be used to design PLED devices with appropriate amount of controlled blending for efficient PLED devices.

Acknowledgement

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