Bi-directional Integrated a-Si Gate Driver Circuit For LCD Panel with RGBW Quad Subpixels

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Abstract: *It is the report on bi-directional integrated a-Si gate driver circuit for LCD Panel with RGBW quad subpixels. RGBW quad subpixels arrangement reduces 1/3 of data lines as well as increases brightness by almost 50%. The direction of vertical scan can change depending on the polarity of two control signals, i.e. Vdd_F and Vdd_R.Iintegrated a-Si gate driver operated over 1,200 hours continuously at 60°C and showed proper operation up to –30°C. Reliability test of gate driver didn't show any dependence on scan direction.*

Keywords: Integrated a-Si gate driver; Bi-directional; RGBW quad arrangement;

Introduction

Integrating driver circuits on the panel is one of fascinating challenges in the LCD industry, because it can reduce total cost, eliminating IC's and its bonding process. Some LCD makers have focused their attention primarily on poly-Si technology for this purpose, because poly-Si TFT gives superior device performance such as higher mobility and more stable device characteristics. The drawback of poly-Si technology is that additional processes are necessary ending up with increasing cost.

Recently, a-Si technology has been improved and several reliable integrated a-Si gate drivers and their driving methods were suggested as a substitution for integrated poly-Si gate drivers or commercial gate-IC drivers (row drivers) on glass substrates from several main AMLCD makers.[1), 2)] Efforts have been also made to reduce the number of data driver ICs.[3), 4)] RGBW quad arrangement is one of them and has the advantage of reducing the number of data driver ICs as well as maximizing aperture ratio.[5)] We have already reported a-Si integrated gate driver for 4.0" QVGA(320×240) panel with RGBW quad subpixels.[6)] A disadvantage of RGBW quad is doubling the number of gate lines, which reduces line select time by 50%. This leads to propagation delays on the gate lines.[7)]

Because integrated a-Si gate driver is based on the a-Si technology, it is easy to put into mass production without extra cost. Therefore the LCDs with integrated a-Si gate driver are expected to be available in the market sooner or later.

In this paper, we present bi-directional integrated a-Si gate driver circuit for LCD Panel with RGBW quad subpixels.

Experimental Detail

A transmissive 7.4" WVGA (720×480) panel with bi-directional integrated a-Si gate drivers has been fabricated using a standard 5-mask process.

RGBW quad subpixels and their driving method

The RGBW subpixels are arranged in a quad structure as shown in Fig.1. A common storage bus is formed between quads to decrease delay on gate line. Because RGBW quad subpixels reduce the number of data lines by one third but double the number of gate lines, the operating frequency increases from 35kHz to 70kHz in WVGA resolutio

There are two sets of integrated gate driver located on opposite side on LCD Panel. Each of them consists of 480 stages of shift register and one dummy stage. One (gate driver A) selects gate lines of odd numbered stages connected to RG subpixels and the other (gate driver B) selects gate lines of even numbered stages connected to BW subpixels. Because each unit gate driver forms on vertically adjoining two subpixels, this driving method provides a merit of saving space with respect to gate driver integration for narrow bezel LCD panel.

Bi-directional Gate Driver

Two control signals and several a-Si TFTs are added to

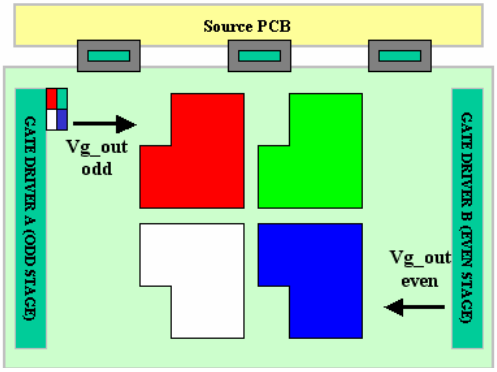

Figure1. Arrangement of quad subpixels and its driving method

our previously reported integrated a-Si gate driver for bi-directional function as shown in Fig.2.[1), 6), 8)] Gate driver is composed of signal bus lines, shifter register and pull-up transistor connected to Q-node and pull-down transistors connected to QB nodes.

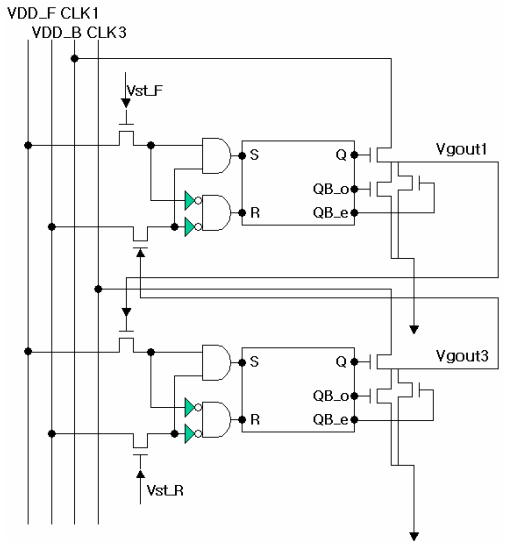

Figure2. Block diagram of integrated a-Si gate driver with bi-directionality

The gate driver was designed to select the direction of operation depending on the polarity of two control signals, i.e. Vdd_F for forward driving and Vdd_R for reverse driving respectively. When Vdd_F and Vst are high and Vdd_R is low, all 480 shift registers are sequentially addressed downward. The direction of addressing is reversed when Vdd_F is low and Vdd_R and Vst are high as shown in Fig.3 and vertical mirror image can be displayed on LCD panel.

To compensate the delay on gate lines resulting from RGBW quad structure, clock signals are extended forward to become overlapped clocks as shown in Fig.3. Overlapped clocks' driving increases charging time of nodes in gate driver and enhances output waveform compared to the normal clocks, which can widen temperature range of proper operation of gate driver despite low mobility of a-Si TFTs. It pre-charges the gate line before the right data signals are transmitted to pixel TFTs of selected gate line. Note that interval between neighboring data doesn't change and data of previous stage is written in overlapped clocks' driving.

Results and discussion

Output waveforms

Our integrated a-Si gate driver continues to transmit the output signal to the last 480th stage up to –30^{o}**C** when operated by overlapped clocks as shown in Fig.4. However, Rise time and fall time increase with decreasing operating temperature. Peak voltage of output waveform at –30 ^{o}**C** doesn't approach the high voltage (VGH) but output waveform is transmitted to the last 480th stage. There is no difference in output waveforms between forward and reverse driving. On the contrary, output waveform disappear at 0^{o}C under normal clock driving. It means that overlapped clocks prevent output waveforms from deteriorating at low temperature by increasing charging time of nodes in gate driver as mentioned previously. However, the exact amount of how many dot clocks are

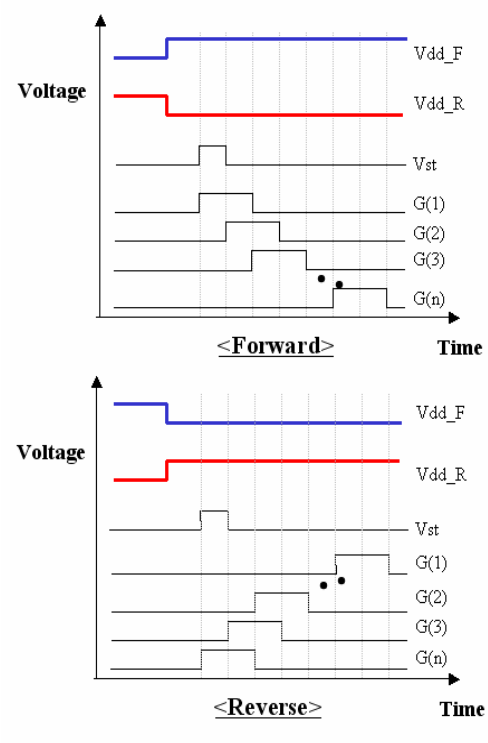

Figure 3 Timing diagram of selecting driving-direction using two control signals; Vdd_F and Vdd_R

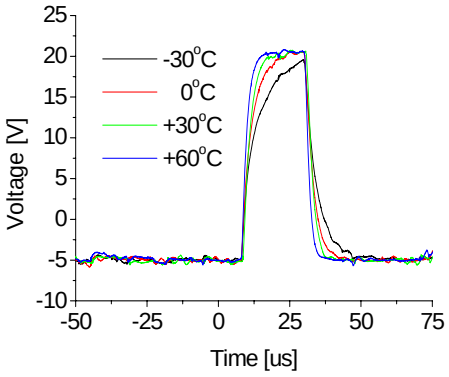

Figure 4 Output waveforms of integrated a-Si gate driver over temperature

overlapped should be optimized case-by-case considering the image quality concerned.

Mobility vs. Temperature

Mobility of a-Si TFT decreases with decreasing temperature as shown Fig. 5. Mobility is 0.55cm^2/Vsec at 30 ^{o}C, but 0.15cm^2/Vsec at –30 ^{o}C. Low mobility at

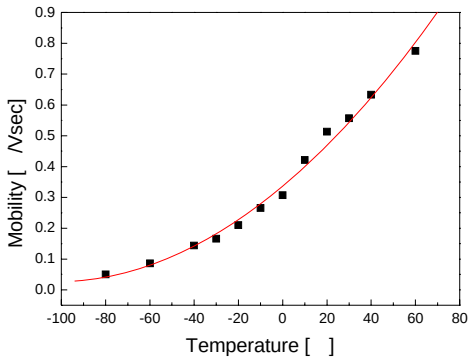

Figure 5 Linear mobility of a-Si TFTs composing gate driver over operating temperature

low temperature means that driving current of pull-up transistor is low and it increases rising time and falling time of output waveform. Because output of previous stage is input signal to next stage, output waveform at low temperature worsens as the output signal is transmitted to downward and finally disappear before it reaches the last stage.

Reliability of gate driver

Clamping voltage has already been suggested as a characteristic voltage to describe a degree of degradation of a driver circuit.[1, 6, 8] It is the minimum applied voltage needed for proper operation of the circuits. The circuit finally becomes mal-functioning when the clamping voltage exceeds the high driving voltage. Fig. 6 shows clamping voltage change over working time at 60**°C,** which is typical of our previously reported DAC a-Si gate driver. It increases at early stage and then levels off after 400 hours to 18V. Bi-directionality doesn't cause any change in clamping voltage over working temperature because bias condition is identically same for both forward and reverse operation.

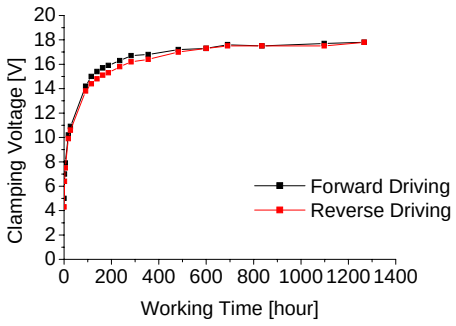

Figure 6 Clamping voltage over working time

Figure 7 Working WVGA panel with integrated a-Si gate drivers

Image of working sample

Fig.7 shows the image of working WVGA panel with integrated a-Si gate driver. It shows good image quality independent of direction of operation.

4. Conclusions

We developed bi-directional integrated a-Si gate driver circuit with RGBW quad subpixels. RGBW quad subpixels arrangement reduces 1/3 of data lines as well as increases brightness by almost 50%. The circuit selects the direction of operation depending on the polarity of two control signals, i.e. Vdd_F for forward driving and Vdd_R for reverse driving respectively. It operated over 1,200 hours continuously at 60°C in both forward and reverse modes and also showed proper operation up to –30°C. WVGA panel with integrated a-Si gate driver also shows good image quality.

Acknowledgement

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