Low-Luminance Square-Pulse Reset Discharge for High-Contrast Drive of PDPs

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Abstract
Although the ramp reset discharge provides a high dark room contrast ratio, it requires a complicated and costly analog circuit. This paper introduces a simple square-pulse reset discharge which takes place between the scan (Y) and address (A) electrodes, unlike the conventional square-pulse reset discharge between the sustain (X) and scan (Y) electrodes. Since the area of the address electrode is smaller than that of the sustain electrode, since the Y-A discharge path is across the two substrates instead of along the front substrate, and also since the Y-A discharge is hidden behind the bus electrode, the light emission is weaker than that of the conventional X-Y square-pulse reset. Background luminance of 0.24cd/m^2 and dark room contrast ratio of 4,600:1 were obtained with the proposed Y-A square-pulse reset discharge technique.

Keywords: plasma display panel; high contrast; square-pulse reset.

Introduction

Improvement of a dark room contrast ratio is important for high picture quality PDPs. This can be achieved by lowering background luminance. A ramp reset waveform is widely used to provide a high contrast [1]. The ramp voltage generator, however, is a relatively complicated and costly analog circuit, and also requires long reset period. In this paper, a technique of low luminance square-pulse reset is proposed in which the reset discharge takes place between the scan (Y) and address (A) electrodes.

Drive Voltage Waveforms

The proposed drive voltage waveforms are shown in Figure 1. A TV-field consists of a reset period and eight subfields. There is only one reset period in a TV-field. Each subfield consists of an address period, a sustain period, and an erase period.

Figure 2 depicts wall charge evolutions during the reset period and the resultant states of discharges just after the changes of the voltages. The timings (1) - (5) in the diagram are also indicated in Fig. 1. Before the reset period, timing (1), no wall charges are accumulated on the electrodes. With applications of reset Y1 pulse and reset D1 pulse whose widths are both 4.0μs, (2), a discharge between the Y and A electrodes occurs, and space charges are generated. These space charges are then accumulated on the walls, (3). At timing (4), a 0.46μs-wide reset Y2 pulse is applied. A Y-A discharge is generated again with an assistance of the wall charges.

At timing (4), a weak X-Y discharge is also generated.

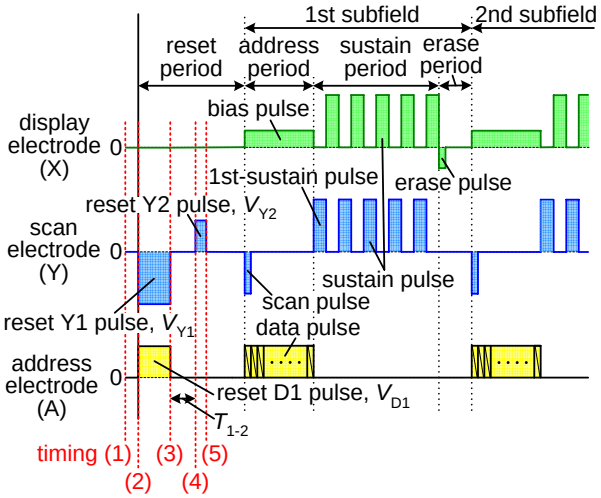

Figure 1. Drive voltage waveforms.

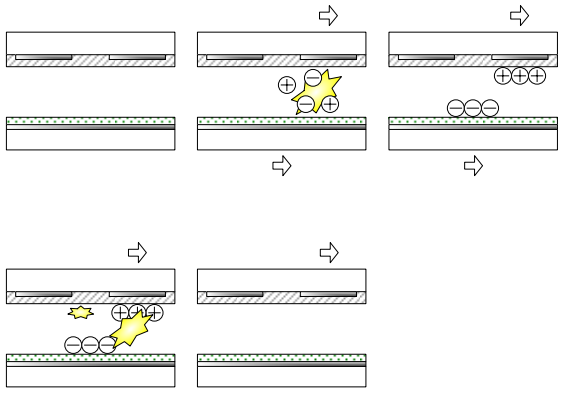

Figure 2. Wall charge evolutions and states of discharges (just after the voltage changes) during the reset period.

All the wall charges are eliminated at timing (5), because the width of the reset Y2 pulse is short enough. The area of the address electrode is smaller than that of the sustain electrode, the Y-A discharge path is across the two substrates instead of along the front substrate, and the Y-A discharge occurs under the bus electrode which blocks the light from the discharge. Therefore the luminance is lower than that of the conventional X-Y square-pulse reset.

The write address scheme [2] is adopted here. For a discharge cell to be ignited (ON cell), a data pulse is applied to generate an address discharge in the address period. The address discharge generates wall charges on each electrode. Then, the sustain pulses continue the discharges. An erase pulse applied after the sustain pulse

eliminates wall charges which have been created during the sustain period. The state of the wall charges after the erase period is made equal to that after reset period. For a discharge cell not to be ignited (OFF cell), no data pulse is applied and hence no address discharge is generated. There are no sustain and erase discharges and there is no change in the state of the wall charges after the subfield. For both ON and OFF cells, the resultant amounts of wall charges are equal to that just after the reset period, namely nil.

Background Luminance

The optimum drive conditions for obtaining the lowest background luminance were experimentally determined using a 7-inch-diagonal, closed-cell-structure, 0.66mm (vertical) and 0.3mm (horizontal) subpixel pitches, Ne+Xe (3.5%) PDP. 72 pixels (9 horizontal lines x 24 RGB subpixels) were sampled.

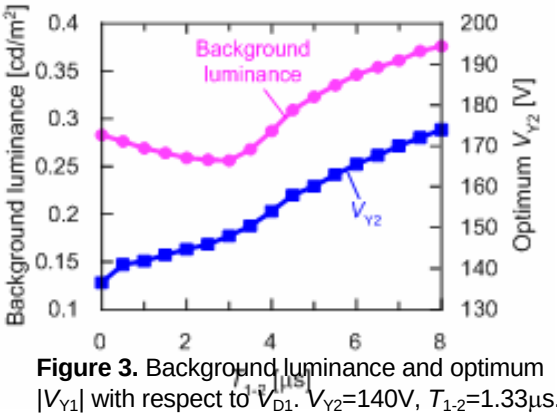

Figure 3. Background luminance and optimum $|V_{Y1}|$ with respect to V_{D1}. V_{Y2}=140V, T_{1-2}=1.33μs.

Figure 3 shows the dependence of background luminance and optimum values of reset Y1 pulse voltage (V_{Y1}) for obtaining the minimum background luminance on the reset D1 pulse voltage (V_{D1}). Here, the reset Y2 pulse voltage (V_{Y2}) and interval between the reset Y1 pulse and reset Y2 pulse (T_{1-2}) were 140V and 1.33μs, respectively. As V_{D1} becomes smaller, $|V_{Y1}|$ increases so that $V_{D1}+|V_{Y1}|$ is kept approximately constant. When V_{D1} becomes smaller than 110V, an undesired discharge is generated between the X and Y electrodes. The background luminance, therefore, increases with the additional discharge.

Figure 4 shows discharge current waveforms through respective electrodes during the reset period. When V_{D1}=70V as shown in Fig. 4 (a), discharge current flows through the X, Y, and A electrodes. With the X-Y discharge, wall charges accumulate on the X electrode. Therefore, the X-Y discharge is also generated with the reset Y2 pulse, resulting in further increase of the background luminance. When V_{D1}=130V, (b), however, no discharge current flows through the X electrode. Thus V_{D1} should be made higher than 110V.

Figure 5 shows the dependence of the background luminance and optimum values of V_{Y2} for obtaining the minimum background luminance on the interval T_{1-2}. Here, V_{D1}=120V and V_{Y1}= -170V were chosen following the results obtained in the previous measurements. Along with an increase of T_{1-2}, V_{Y2} increases since the space charges produced by the reset D1 pulse decrease [3]. The background luminance, however, decreases since excessive current flow is limited by the space charges. The lowest luminance is obtained when T_{1-2}=3.0μs. When T_{1-2} is longer than 3.0μs, V_{Y2} has to be made higher, resulting in a generation of intense discharges, resulting in higher background luminance. It should be noted that, in Ne+Xe (3.5%) PDPs, the decay time of the space charges is of the order of 3μs [4] which corresponds to the optimum T_{1-2}.

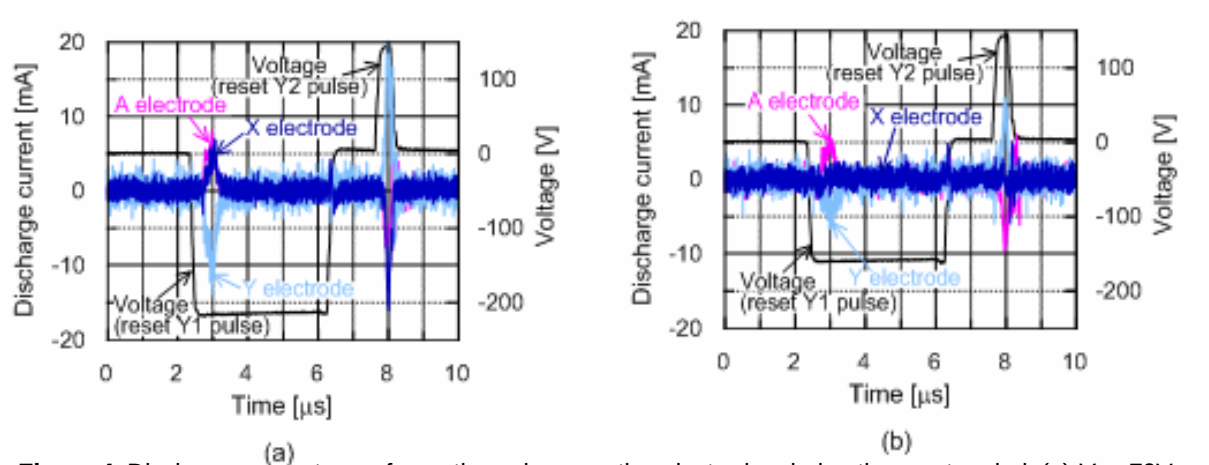

Figure 4. Discharge current waveforms through respective electrodes during the reset period. (a) V_{D1}=70V, both X-Y discharge and Y-A discharge are generated. (b) V_{D1}=130V, only Y-A discharge is generated.

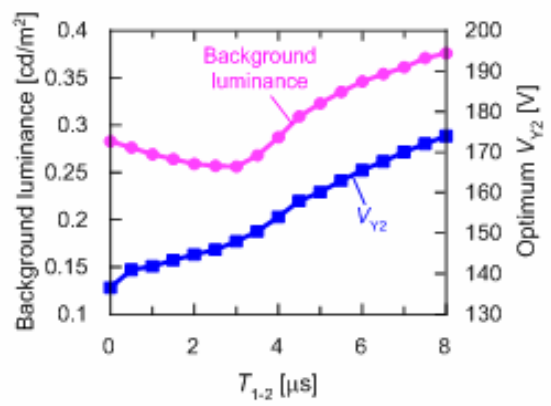

Figure 5. Background luminance and optimum V_{Y2} with respect to T_{1-2}. V_{D1}=120V, V_{Y1}= -170V.

Further Reduction of Background Luminance

In order to reduce the background luminance further, the X-Y discharge generated at timing (4) of Figs. 1 and 2 should be suppressed. This has been achieved by adding a reset X2 pulse corresponding to the reset Y2 pulse, as shown in Fig. 6 (a). Figure 6 (b) shows the dependence of the background luminance on the reset X2 pulse voltage (V_{X2}). Here, V_{D1}, V_{Y1}, V_{Y2}, and T_{1-2} were 120V, -170V, 150V, and 3.0μs, respectively. As V_{X2} increases, the background luminance decreases as a result of suppressed X-Y discharge. When V_{X2} exceeds 40V, however, an X-A discharge is generated, increasing the background luminance. When V_{X2} is higher than 160V, the background luminance becomes higher than that when the reset X2 pulse is not applied (V_{X2}=0V). The optimum value of V_{X2} is 40V, when the lowest luminance of 0.24cd/m^2 is obtained.

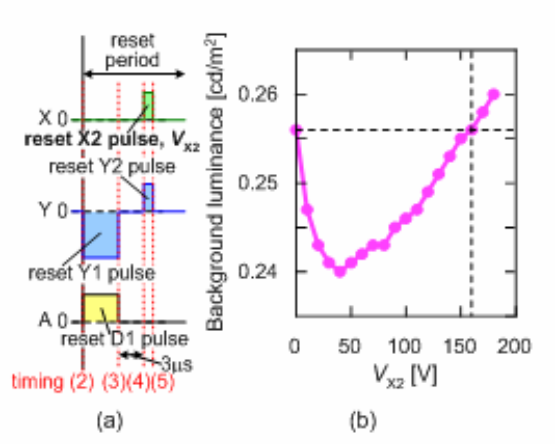

Figure 6. Addition of reset X2 pulse on the X electrode. (a) Drive voltage waveforms during the reset period. (b) Background luminance *vs.* V_{X2}. V_{D1}=120V, V_{Y1}= -170V, V_{Y2}=150V and T_{1-2}=3.0μs.

Phosphor Lifetime

In the proposed Y-A square-pulse reset discharge waveforms of Figs. 1 and 6, the address electrode becomes cathode when the reset Y2 pulse is applied. The ions then bombard with phosphor, possibly degrading the phosphor to some extent. In the write address drive scheme, the address electrode also becomes the cathode when the first sustain pulse on the scan electrode is applied, resulting in possible phosphor damage. This damage takes place even when the ramp reset discharge is employed.

Figure 7 (a) shows the discharge current through the A electrode when the reset Y2 pulse is applied. For comparison, discharge current with the 1st-sustain pulse is shown in (b). In (a), the peak discharge current is high, but the discharge terminates within 0.3μs. On the other hand, in (b), peak discharge current is about 1/3, but the discharge lasts for 1.5μs. The total charge flow for both cases, calculated by integrating the discharge current with respect to time, is 0.6nC for (a) and 1.3nC for (b).

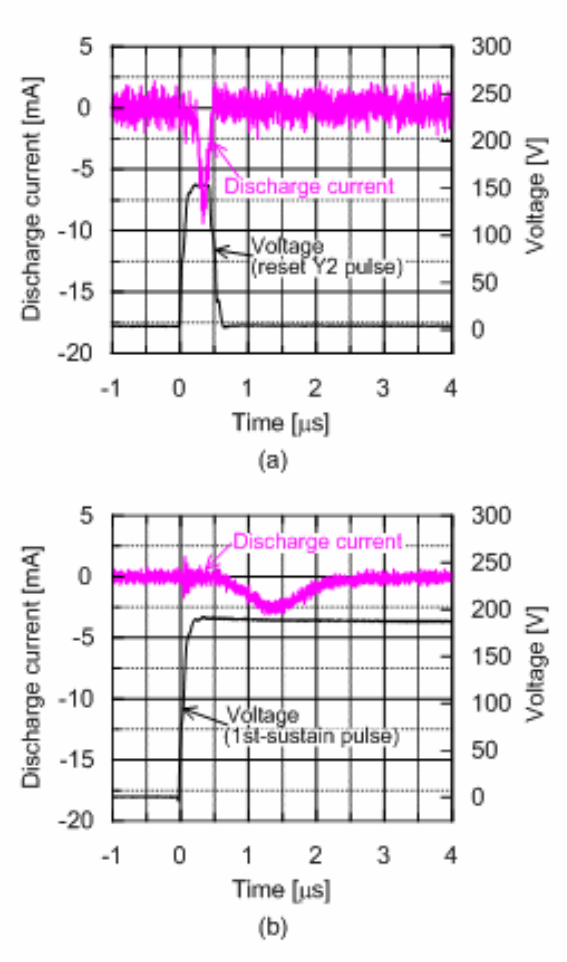

Figure 7. Discharge current waveforms through the address electrode. (a) During reset Y2 pulse. (b) During 1st-sustain pulse on Y electrode. Each pulse is applied at time 0.

If an 8-subfield drive is assumed, then, with a ramp reset and eight 1st-sustains, the total charge flow to the address electrode becomes approximately 1.3x8=10.4nC. With the Y-A square-pulse reset and eight 1st-sustains, the total charge flow is 1.3x8+0.6=11nC, only 6% larger than with the ramp reset, implying that the phosphor damage would not be increased much.

In order to investigate further the phosphor damage, luminance variation is being observed. At the elapsed time of 1,000 hours, no difference in the luminance degradation is found for the conventional X-Y square-pulse reset and the proposed Y-A square-pulse reset.

Peak Luminance

Table 1 shows peak luminance in white, background luminance, and dark room contrast ratio for the conventional X-Y square-pulse reset, ramp reset, and proposed Y-A square-pulse reset. One reset period and eight subfields were provided in a TV-field. The active area of 9x8 pixels consisted of a portion of a 640 x 480-pixel VGA panel, with a dual scan operation.

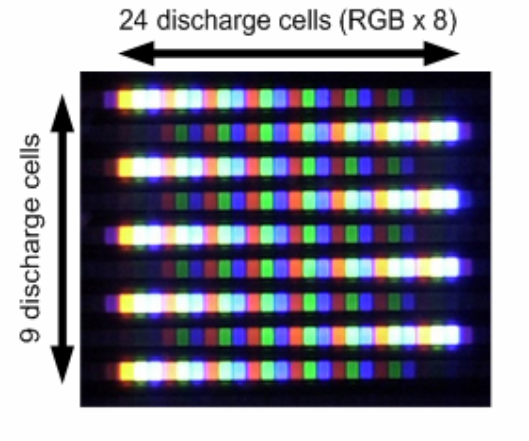

Figure 8. Gradation pattern expressed on a Ne+Xe (3.5%) panel (9x24 discharge cells).

The dark-room contrast ratios for these three cases were 2,600:1, 6,900:1, and 4,600:1, respectively. The peak luminance was 1,100cd/m^2. Figure 8 shows a gradation pattern of the test panel.

Conclusions

A low luminance square-pulse reset technique has been proposed in which the reset discharge takes place between the scan (Y) and address (A) electrodes. The reset pulse voltages should be optimized so that they do not initiate X-Y discharges. The proposed Y-A square-pulse reset improved the dark room contrast ratio by a factor 1.8 over the conventional X-Y square-pulse reset, although the contrast is lower than that of the ramp reset by a factor 1.5. The dark room contrast ratio of 4,600:1, however, can be considered acceptable. The complicated ramp voltage generator can be eliminated with the present technique.

Acknowledgments

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Table 1. Panel drive conditions and performances for respective reset waveforms. A VGA panel with dual scan operation is assumed.

Reset waveforms	Conventional X-Y square-pulse reset	Ramp reset	Proposed Y-A square-pulase reset
Width of reset period	15.5μs	250μs	14.6μs
V_{data}	70V	100V	140V
V_{scan}	-150V	-111V	-150V
$V_{sustain}$	190V	185V	190V
Peak luminance (white)	1100cd/m^2	1100cd/m^2	1100cd/m^2
Background luminance	0.43cd/m^2	0.16cd/m^2	0.24cd/m^2
Dark room contrast ratio	2600:1	6900:1	4600:1