Temperature dependence on the hysteresis of a-Si:H TFT and Elimination of the hysteresis effect on OLED current for AMOLED Display

Sang-Geun Park, Jae-Hoon Lee, Won-Kyu Lee, and Min-Koo Han*
School of Electrical Engineering and Computer Science #50, Seoul National University
San 56-1, Shillim-Dong, Kwanak-Gu,151-742, Seoul, Korea
*mkh@ snu.ac.kr

Abstract: *The temperature dependence on the hysteresis of a-Si:H TFT has been investigated. We have also proposed and fabricated a new a-Si:H TFT pixel driving scheme, which can eliminate OLED current error caused by the hysteresis of a-Si:H TFT. At an elevated temperature from 25°C to 60°C, the V_{TH} variation of a-Si:H TFT caused by hysteresis was decreased from 0.41V to 0.17V due to an increase of s-slope, which was caused by an increase of initial trapped charge. Although OLED current variation caused by hystereis was decreased (~14%) as a temperature was increased, the OLED current error needed to be improved for driving pixel circuit of AMOLED. In the proposed circuit, the reset voltage (-10V) was applied before a data voltage for a present frame was written, so that the sweep direction of data voltage was fixed, resulting in the elimination of hysteresis effect on OLED current. The variation of OLED current was successfully suppressed in the proposed pixel circuit regardless of an operating temperature.*

Keywords: a-Si:H TFT; hysteresis; AMOLED.

Introduction

Active matrix organic light emitting diode (AMOLED) employing thin film transistor (TFT) pixels, such as amorphous or polycrystalline silicon TFT, have attracted considerable attentions due to high brightness, compactness and wide viewing angle [1-2]. Recently, hydrogenated amorphous silicon (a-Si:H) TFTs are considered as the pixel element of AMOLED due to high uniformity in large areas. However, it is well known that threshold voltage of a-Si:H TFT is easily increased due to electrical bias stress [3-8].

Hysteresis phenomenon of a-Si:H TFTs needs to be improved for a high quality AMOLED circuit. Residual image due to the hysteresis phenomenon of a-Si:H TFT, such that the previous display image remains apparent in the subsequent image, may be problem observed in conventional TFT pixel composed of 2-TFT. We recently reported a-Si:H TFT device studies, showing that the hysteresis of a-Si:H TFT can make OLED current variation at room temperature, when an identical data voltage is applied to a-Si:H TFT pixel [9]. However the temperature dependence on the hysteresis of a-Si:H TFT was not investigated in the previous work. Because an actual operating temperature of AMOLED panel is much higher than the room temperature, the investigation of the temperature dependence on the hysteresis of a-Si:H TFT is required.

The purpose of our work is to investigate the temperature dependence on the hystresis of a-Si:H TFT in order to study the hysteresis effects on OLED current. We have also proposed a new pixel driving scheme to eliminate OLED current variation caused by the hysteresis of a-Si:H TFT. Our experimental results show that under the proposed pixel driving scheme, OLED current variation caused by the hysteresis can successfully be eliminated due to the fixed V_{GS} sweep direction of a-Si:H TFT at both room temperature and at an elevated temperature to 40°C.

Experiment

The a-Si:H TFT with an inverted staggered bottom gate type was fabricated employing a standard commercial process as shown in Fig. 1. Triple layer of SiN_x (450nm), a-Si:H (200nm), n+ a-Si:H (50nm) was deposited by plasma-enhanced chemical vapor deposition (PECVD) after gate patterning. Active island, source and drain electrode were patterned on the deposited triple layer. After patterning the source and drain electrode by a wet etching, the n+ a-Si layer between the source and drain electrode was removed by a dry etching to make an etch back type channel structure. 300nm thick SiN_x was deposited for a passivation. After contact holes are formed, an indium tin oxide (ITO) electrode was deposited and patterned. The transfer characteristics of device were measured by HP4156 semiconductor analyzer at various temperatures in order to investigate the temperature dependence on the hysteresis of a-Si:H TFT.

The novel AMOLED driving circuit to suppress hysteresis was designed and fabricated employing a-Si:H TFT. The circuit was measured at various temperatures in order to verify that the proposed circuit can suppress the hysteresis characteristics of a-Si:H TFT regardless of an operating temperature.

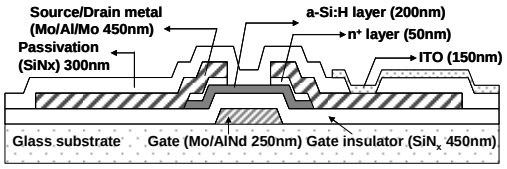


Figure 1. The cross-section view of fabricated bottom gate a-Si:H TTFs

Results and Discussion

Fig. 2. shows the measurement results of transfer characteristics of a-Si:H TFT at 25°C and 60°C respectively. When a temperature was 25°C, the

threshold voltage of forward voltage sweep direction (increasing gate voltage) was 2.14V while that of reverse voltage sweep direction (decreasing gate voltage) was 2.55V due to hysteresis of a-Si:H TFT. When a temperature was 60°C, the threshold voltage of forward voltage sweep direction was 1.84V while that of reverse voltage sweep direction was 2.06V.

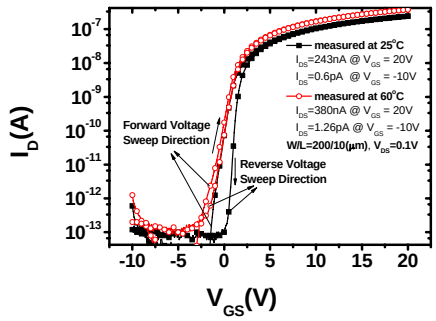


Figure 2. The transfer characteristics of a-Si:H TFT.

In order to investigate the temperature dependence on the hysteresis of a-Si:H TFT, the s-slope of a-Si:H TFT was measured at various temperatures from 25°C to 60°C as shown in Fig. 3. The s-slope ($dV_G/d(\log I_D)$) of reverse voltage sweep direction is smaller than that of forward voltage sweep direction, because the trapped electron charges at reverse sweep direction are released faster than trapped hole charges at forward sweep direction. As a temperature was increased, the s-slope of a-Si:H TFT was also increased due to an increase of initial trapped charges. However the s-slope of reverse voltage sweep direction was increased more than that of forward voltage sweep direction, resulting in a decrease of hysteresis. The s-slope of reverse voltage sweep direction was increased from 0.24 V/decade to 0.59 V/decade while that of forward sweep direction was increased form 0.55 V/decade to 0.64 V/decade as a temperature was increased.

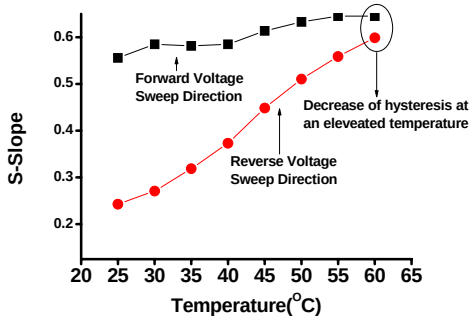


Figure 3. The measured s-slope of a-Si TFT at various temperatures.

The s-slope of each voltage sweep direction such as forward or reverse sweep direction, was increased differently due to different change of hole current and on current. As shown in Fig. 2. the hole current at low gate voltage was not much increased while the on current was increased significantly as a temperature was increased. The hole current was increased only 0.66pA at an elevated temperature (60°C). Although a temperature was elevated up to 60°C, less quantity of hole charges gained thermal energy than electron charges due to heavier mass, and almost hole charges were blocked by n+ layer, so the hole current was not much increased. Initial trapped hole charges were not increased almost at forward voltage sweep direction due to a small increase of hole current even at an elevated temperature (60°C). However on current was increased about 137nA at an elevated temperature (60°C) due to an increase of electron carriers, which gained thermal energy. Much more electron charges were trapped at 60°C than at 25°C due to an increase of on current, so the s-slope of reverse voltage sweep direction was more increased than that of forward voltage sweep direction. The trapped charges may be released by gate voltage, so that the de-trapping rate of trapped charges might not be altered by an elevated temperature. The s-slope of the reverse voltage sweep direction was increased more than that of the forward voltage sweep direction due to the initial trapped charges. The initial trapped charges at each voltage sweep direction are shown in Fig. 4. and Fig. 5. respectively.

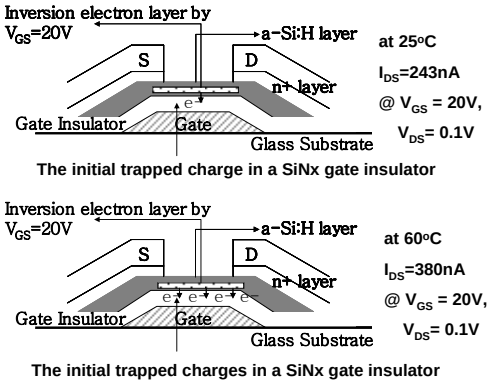


Figure 4. The initial trapped electron charges at reverse voltage sweep direction. Much more electrons are trapped in gate insulator at 60°C than at 25°C.

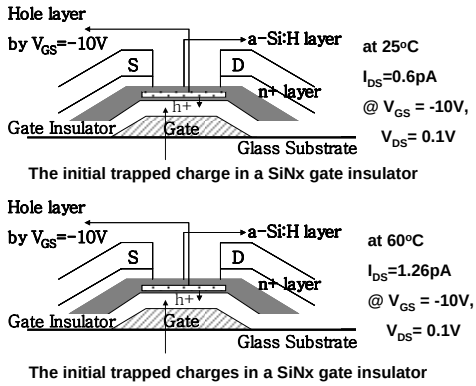


Figure 5. The initial trapped hole charges at forward voltage sweep direction. The initial trapped hole charges are not increased almost at 60°C.

In order to investigate the relation between an observed hysteresis and OLED current error, we have measured a

current with different starting gate-voltage in a-Si:H TFT. Fig. 6 is the output current variation in the a-Si:H TFT with a different starting gate-voltage, from 0V to 8V. Fig. 6 shows that the same gate-source (V_{GS}=4V) and drain-source (V_{DS}=10V) voltages exhibits the different output current with the previous gate-source voltage due to hysteresis phenomenon with a different starting gate-voltage. For example, the drain current of 1.67μA was measured at a previous gate-source voltage of V_{GS}=0V, while that of 1.46μA was measured at a previous gate-source voltage of V_{GS}=8V. When the voltage sweep direction is fixed, the OLED current may not be altered in the AMOLED circuit.

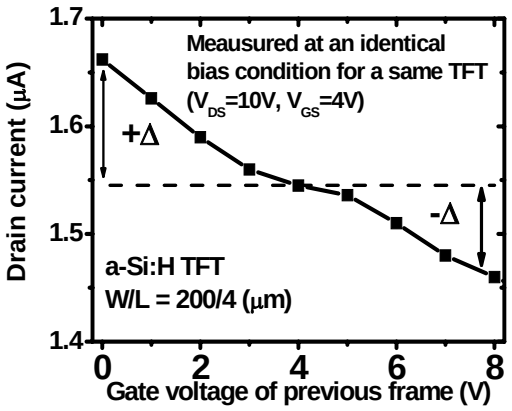
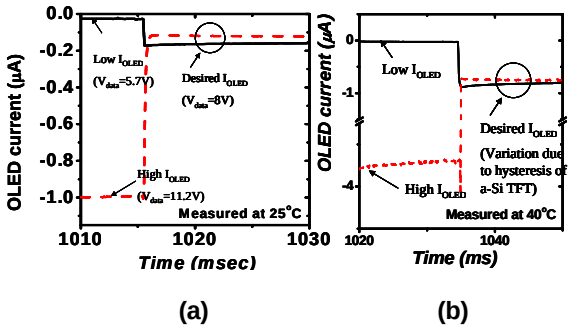


Figure 6. Experimental results of the drain current at the identical V_{GS}, V_{DS}, with previous gate starting voltage at the identical a-Si:H TFT device.

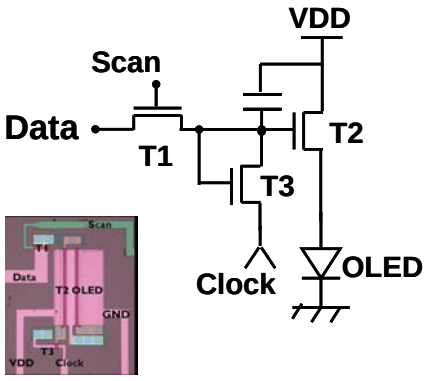
The measurement results of conventional 2-TFT pixel circuit at 25°C and 40°C are shown in Fig. 7(a) and Fig. 7(b) respectively. Although the hysteresis of device at high temperature was smaller than at room temperature, the OLED current was altered. When we applied data voltage of 8V to conventional 2-TFT driving pixel circuit, the OLED current was altered according to previous data voltage due to hysteresis of a-Si:H TFT. The OLED current, which was determined by data voltage of 8V, was altered from 119nA to 164nA according to the previous data voltage at 25°C. The OLED current variation ((I_{HIGH}-I_{LOW})/I_{LOW}X100) was about 38%. When the OLED current was measured at 40°C, the OLED current was altered form 0.74μA to 0.84μA according to previous data voltage even at the same data voltage. The OLED current variation was about 14% at 40°C. While the variation of OLED current was decreased as a temperature was increased, it was too large (~14%) to be applied for high quality AMOLED display. As shown in Fig. 6. if the voltage sweep direction of a-Si:H TFT is fixed, an OLED current variation might be eliminated.



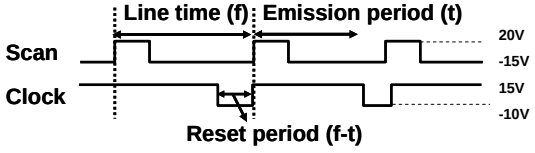
(a) (b)

Figure 7. The measurement result of OLED current in the conventional 2-TFT pixel circuit. (a)The measurement result of OLED current at 25°C (b) The measurement result of OLED current at 40°C. The current variation is reduced slightly at 40°C.

We have proposed a novel 3-TFT driving circuit to eliminate OLED current variation caused by hysteresis of a-Si:H TFT. In the proposed 3-TFT driving circuit, an OLED current variation was eliminated by fixing the voltage sweep direction. The proposed driving circuit was fabricated and measured. The schematic of the proposed pixel circuit and microscopic picture of fabricated circuit are shown in Fig. 8(a). The diode connected TFT and parallel capacitor were used to evaluate OLED current. The gate length of T1, T2 and T3 is 4μm. The channel width of driving TFT, T2 is 200μm to make enough current to OLED device. The channel width of T1 and T3 is 35μm and 8μm respectively. The parasitic capacitance for OLED was fabricated as 2pF.



(a)



(b)

Figure 8. The schematic of the proposed 3-TFT pixel circuit to eliminate OLED current variation. (a)The schematic of a proposed pixel circuit and microscopic picture of a fabricated pixel circuit. (b)The time diagram of signals.

The measurement results of the proposed 3-TFT circuit at 25°C and 40°C are shown in Fig. 9(a) and Fig. 9(b) respectively. At both temperatures the OLED current in the proposed 3-TFT pixel circuit was not altered regardless of previous data voltage. The detailed signal parameters, such as scan signal and clock signal are shown in Fig. 8(b). When a clock signal is high, T3 is turned off due to V_{GS}_T3=0 so that OLED current flows from V_{DD} to OLED by a data voltage. After OLED current flows, a clock signal goes down to -10V, and the negative voltage is applied to gate node of T2, so that OLED current is 0A. Before the data voltage is applied to gate node of T2, the negative reset voltage is applied to gate node of T2. The voltage sweep direction of driving TFT is fixed as forward voltage sweep direction regardless of the previous data voltage. The OLED current error caused by a-Si:H TFT hysteresis is successfully eliminated in the proposed pixel circuit.

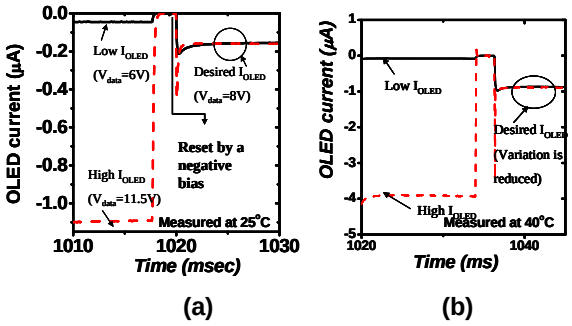


Figure 9. The measurement result of OLED current in the proposed 3-TFT pixel circuit. (a)The measurement result of OLED current at 25°C. (b) The measurement result of OLED current at 40°C.

Conclusion

We have investigated the temperature dependence on the hysteresis of a-Si:H TFT. The hysteresis of a-Si:H TFT was decreased as a temperature was increased because at an elevated temperature from 25°C to 60°C, the s-slope of a-Si:H TFT at reverse voltage sweep direction was increased more than at forward voltage sweep direction due to an increase of initial trapped electrons in a gate insulator.

When a-Si:H TFT is used as a pixel element of AMOLED, the variation of current caused by hysteresis of a-Si:H TFT might cause some problems such as residual images. Although the same data voltage is applied, the OLED current is altered according to the previous data voltage due to hysteresis of a-Si:H TFT.

We have successfully designed and fabricated a novel 3-TFT driving circuit to eliminate OLED current variation. When we applied data voltage of 8V to conventional 2-TFT pixel circuit at room temperature, the OLED current was varied from 119nA to 164nA according to previous data voltage. Although the OLED current variation was reduced (~14%) when it was measured at 40°C, it needed to be improved to drive pixel circuit. In the proposed pixel circuit, negative reset voltage is applied before present data voltage is written, so that OLED current is not altered. Our experimental results show that OLED current variation was eliminated in the proposed 3-TFT circuit both at room temperature and at 40°C.

The proposed pixel circuit may be suitable for high quality AMOLED display.

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