New Active Pixel Design Using μc-Si TFT Technology for AM-OLED Backplane

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Abstract: *In this paper, we propose and fabricate a new active pixel circuit design integrated on active-matrix organic light-emitting diode (AMOLED) display. Moreover, we have developed a thin film transistor (TFT) based on microcrystalline silicon (μc-Si) active layer for a more efficient process and a better uniformity of driving transistor characteristics. The experimental results show that the emission current uniformity is improved in contrast to the conventional 2-TFT pixel circuit. Thus the proposed averaging driver successfully improves the inter-pixel uniformity.*

Keywords: Active-matrix organic light-emitting diode (AMOLED); thin film transistor; current driving; organic light-emitting displays; microcrystalline silicon *(μc-Si)*.

Introduction

Fast response time, high efficiency or light weight are some attractive merits achievable using active-matrix organic light-emitting diode (AMOLED) display technology. Since the luminance of the display is proportional to the driving current delivered to the diode, the pixel circuits must be carefully designed to supply a constant current during each frame period. The use of low-temperature polycrystalline silicon (LTPS) TFT or hydrogenated amorphous silicon (a-Si:H) TFT as backplanes to drive OLED are actually the more mature manufacturing technologies. However non-negligible TFT characteristic fluctuations are observed consecutively to the fabrication process variations or the device aging. Crystallization of amorphous silicon from excimer laser annealing (ELA) is a widely-used method in LTPS. Nevertheless this technique suffers from laser shot-to-shot instability of energy resulting in random variation of both field effect mobility and threshold voltage (V_T) parameters. On the other side, the variable gate-bias on a-Si:H drive TFT lead to uncontrollable gate-insulator trap density that induces significant V_T-shift especially in time. Moreover a-Si:H provides low TFT mobility, resulting in an increased display power consumption and limited pixel aperture ratio.

Among the different driving schemes and pixel designs that have been suggested to relieve image degradations [1-4], two approaches are mainly used for pixel addressing : voltage or current driven circuits. The diode-connected drive TFT or the current reproduction method are well known compensation techniques but require additional lines, TFT or specific drivers resulting in complicated designs or addressing schemes.

In this paper, we present an improved voltage input pixel circuit based on microcrystalline silicon (μc-Si) TFT technology introducing an averaging function. A multiple driving TFT structure is proposed here to statistically overcome the inter-pixel non-uniformity issue. The proposed design can also improve the OLED current distribution inside each pixel element. First, we describe our experimental procedure and the operation principles of the pixel circuit. Next, the non-uniformity of the driving current is evaluated on an AMOLED backplane.

Device and pixel circuit realization

Microcrystalline silicon

Microcrystalline silicon films are preferentially deposited by conventional plasma enhanced chemical vapour deposition (PECVD) at low temperature (≤300°C) and is being considered as a solution for flexible electronic devices [5-6]. High performance using this material has been reported but reproducibility and reliability are under development. Our approach is to achieve better performance and immunity than conventional a-Si:H technology. Thus our silicon films are directly deposited into crystallized state at 600°C and 0.1-Pa on silicon dioxide covered glass substrate in a standard low-pressure-CVD reactor. At such high temperature the material is free from hydrogen and it can be highly stable. Silicon deposition conditions result in a microcrystalline material with small-sized grains and on average a diameter around 50-nm. XRD measurements of this material show [220] preferential orientation, contributing with the small grain size to the uniformity.

Backplane fabrication based on μc-Si TFT process

Figure 1. shows an active pixel circuit structure based on an in-house μc-Si-monolayer-TFT process by eight-mask steps and two shadow masks for AMOLED realization.

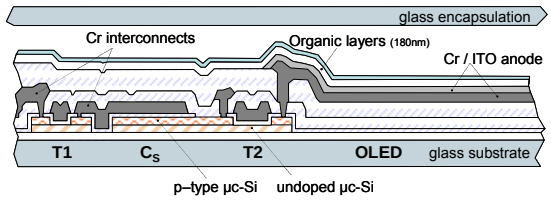

Figure 1. Schematic diagram of an active-pixel integrating top-gate p-type μc-Si TFT and top-emitting OLED structure.

First a 250 nm-thick buffer silicon oxide is deposited on glass substrate using an atmospheric-pressure-CVD

(APCVD) system. Subsequently a 150-nm intrinsic µc-Si layer is deposited followed without interruption by 150-nm heavily boron doped film by low-pressure-CVD (LPCVD). After active islands definition, P+ regions and capacitor electrode are defined. Then, a 70-nm-thick SiO_2 gate insulator layer is deposited at 430°C by APCVD. The devices were then furnace annealed at 600°C for at least 1h in order to perform SiO_2 and interface quality. The gate oxide was patterned and wet etched by buffered oxide etch solution. Then, 350-nm chromium films are deposited by evaporating method and patterned to form source/drain contacts, row/column and gate electrode. As the TFT fabrication completed, a 450nm SiO_2 passivation layer was then deposited and a via was opened down to the chromium/ITO electrode. The ITO layer was sputter deposited and defined for the bottom anode contact. Once the backplane was fabricated, a hole injection layer, a green light emissive layer and an electron transport layer were evaporated through a shadow mask. Finally, a thin semitransparent bi-layer cathode for top-light emitting (Fig. 1), was thermally evaporated through another shadow mask without breaking vacuum. The active matrix fabrication was finished by a simple glass encapsulation used to prevent OLED device from moisture and oxygen diffusion degradation.

Furthermore, by using the same equipment, p-type poly-Si TFT have been fabricated with the same process to compare the influence of material on electrical uniformity. Thus, LPCVD deposited amorphous silicon film is crystallized by solid phase crystallization (SPC) using standard furnace-annealed amorphous silicon process at 600°C for 10-h in vacuum. Contrary to laser-annealed polysilicon, a better spatial uniformity is expected due to a simultaneous crystallization of amorphous silicon layer.

Microcrystalline silicon TFT characteristics

Figure 2 shows the electrical characteristics of ten neighbour µc-Si TFT used for selecting and switching. Extracted maximum field-effect mobility and threshold voltage from those characteristics are 5,9cm² V^{-1} s^{-1} and –8.3V respectively. Some driving TFT parameters are summarized in Table I.

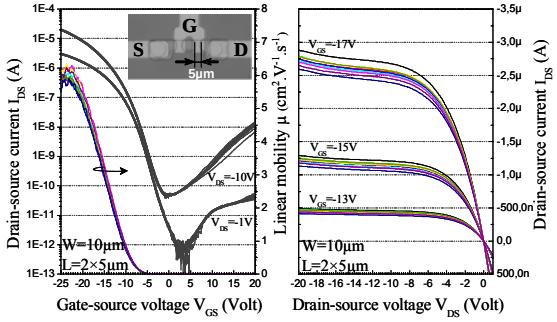

Figure 2. Transfer, linear mobility and output characteristics of 10 neighbour dual-gate µc-Si TFTs used for data-switching operation (maximum distance : ~3mm).

Table 1. Typical p-channel µc-Si TFT parameters used to supply OLED current

Gate oxide thickness	70nm
Threshold voltage V_T	-8.5V
Linear mobility μ_L ($cm^2.V^{-1}.s^{-1}$)	5.9
Saturation mobility μ_S ($cm^2.V^{-1}.s^{-1}$)	3.4
Leakage current I_{OFF}	<10pA(V_{DS}=-5V)
Driving TFT width/length (W/L)	36µm / 20µm

Driving µc-Si-TFT in our pixel electrode circuits are obviously able to provide up to 10µA for rather low V_{GS} and V_{DS} (less than 20V) and with small channel dimensions.

New voltage programmed active pixel circuit design

Multiple drive TFT technique

Designs of both conventional 2-TFT active pixel circuit and proposed one are shown in Figure 3. Both designs contain a switching TFT T_1 and an OLED driving TFT T_2 acting as a voltage controlled current source and used to convert an input data voltage to a constant current. When the pixel is turned on, the pixel state is sustained during one frame period by the storage capacitor C_S. Two TFTs are the minimum required for the standard active pixel design. The new design consists on several distributed sources with a specific layout on the pixel area. From our experiments, a local distribution of drive TFT inside a pixel has shown a significant reduction of driving current dispersion from six distinct channels. A further improvement is expected by taking into account the whole pixel area. Indeed grain size changes and local variations due to the fabrication process (etching and plasma, residues…) or inhomogeneous layers favour spatial non-uniformity. In the present study, three TFTs are provided as driving elements. Each TFT is divided into two channels with a double gate structure. A simple geometry of OLED anode pattern is desirable, especially when using bottom emission, in order to prevent thickness variations of organic layers or misalignments. Therefore, a better display uniformity is expected without additional restrictions.

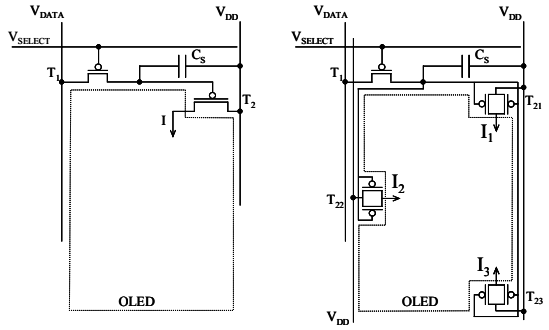

Figure 3. Designs of a conventional pixel element (left) and proposed circuit integrating a spatial distribution of driving current. Here, only three

distinct areas are chosen in order to preserve aperture ratio in case of a bottom light emission.

Driving channels are connected in parallel and the total current flowing through a driving TFT during emission period is expressed by

$$I_{OLED} = \sum_{i=1}^{n} \frac{W}{2nL} \times \frac{\varepsilon}{d_{OX}} \times \mu_i \times (V_{GS} - V_{Ti})^2 \quad (1)$$

where μ_i is the local channel field effect mobility, V_{Ti} the threshold voltage, V_{GS} the applied source-gate voltage and W, L the channel width and length respectively. The capacitance per unit area of the gate oxide $C_{OX}=\varepsilon/d_{OX}$ is locally considered as a constant ($\Delta d_{OX} \leq 2\%$ per cm²). Consequently the current depends only on V_T and μ_{FE} fluctuations. The supplied OLED current is the sum of individual currents. Thus, using equation (1), a global expression of this current can be formulated :

$$I'_{OLED} = \frac{W}{2nL} C_{OX} \times \left[\sum_{j=1}^{m} \sum_{i=1}^{n} \mu_i \times (V_{GS} - V_{Ti})^2 \right] \quad (2)$$

where m is the number of driving transistors per pixel and n is the number of channels per transistor. The standard deviation can then be obtained :

$$\sigma_{OLED} = \frac{W}{2L} C_{OX} \times \sigma \left[\sum_{j=1}^{m} \sum_{i=1}^{n} \frac{1}{n} \times \mu_i \times (V_{GS} - V_{Ti})^2 \right] \quad (3)$$

This relation suggests a design of drive transistors with a high density of channels. Nevertheless, multi-channel TFT design involves higher circuit area that have to be taken into account in case of bottom light emission.

Evaluation of electrical uniformity

Figure 4. shows an optical micrograph of pixels arranged in an active-matrix configuration, each having the above-described architecture. Three contact pads are designed inside each sub-pixel to evaluate current waveform during operation. An ITO-anode is deposited later to cover entirely these pads. All electrical measurements of pixel circuits are performed at room temperature directly on active matrix using a probe station. Pulse signals as V_{DATA} and V_{SELECT} are applied by a pulse generator unit (HP41501A) with a duty cycle of 5% (On time: 1ms, Off time: 19ms). The power voltage V_{DD} (source of driving-TFT) and output signals are controlled by a semiconductor parameter analyser (HP4155B).

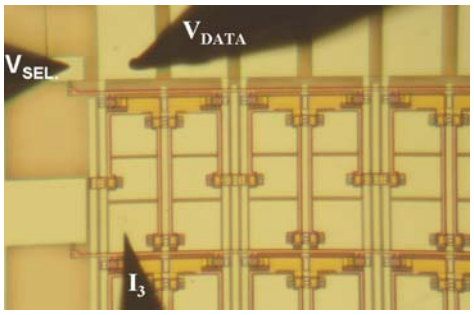

Figure 4. Top-view of the fabricated active pixel circuits using a stripe arrangement in the processed backplane before OLED stack (sub-pixel pitch: 160×415µm²).

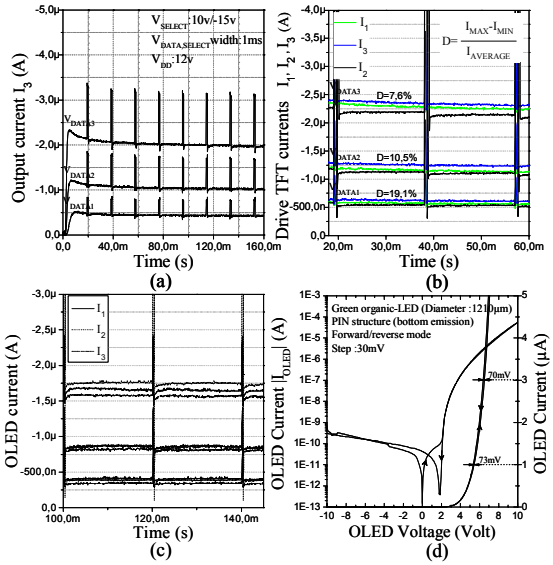

Figure 5. Transient measurements of (a) I_3 current during several frame times highlighting C_S reset effect (b) current levels disparity inside one pixel (c) OLED currents obtained from a diode connected to a circuit (d) I-V forward/reverse characteristics of test green-OLED used to evaluate circuits

Figure 5.a shows the output current I_3 plotted versus time for several values of data signal with the driving TFT drain grounded. Asynchronous signals (Δt=500µs) are applied here to evaluate discharge effect. Voltage drop through capacitor involves high output current during programming time (+50%). Note that current also rise using synchronous signals, Fig. 5b. (gate overlaps are here close to 2µm). Nevertheless using an OLED connected in series with the driving TFT no light flash was observed despite the short response time of the diode, due to the brief duration of impulsions. Furthermore, OLED current variations inside each circuit are obvious (Fig.5b-c) and have been observed on a large majority of pixels. Current variations of 15 pixels measured along a column and addressed to deliver the same current level are shown in Figure 6. Each individual

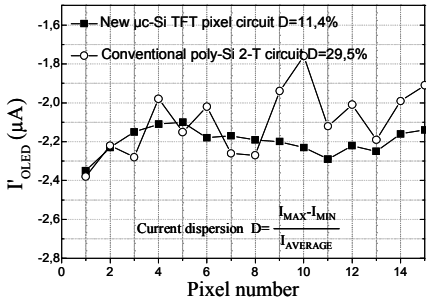

Figure 6. Dispersion of output current along one column using proposed µc-Si-pixel design compared to conventional 2-TFT circuit based on polysilicon active layer.

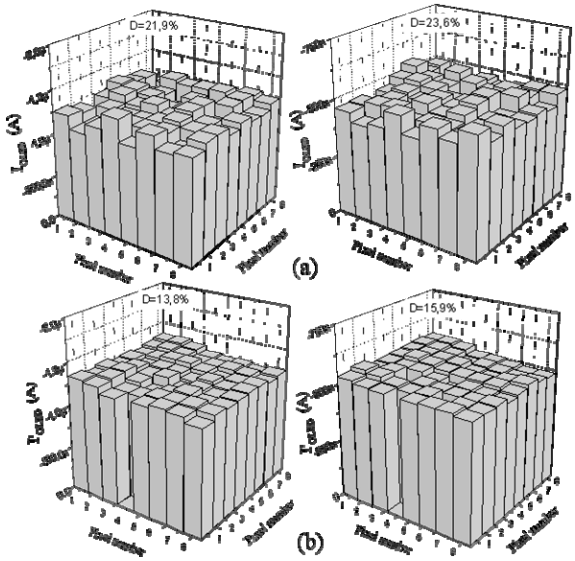

Figure 7. Spatial representations of currents using conventional 2-TFT pixel circuits based µc-Si active layer (a). The same measurements are achieved using proposed pixel circuit design (b). Measurements are performed on 8×8 neighbour pixels (V_{DS}=-5V,V_{DD}=10V). It can be seen that proposed circuit is more uniform.

current is measured at 10ms of a sampling time after the scan signal is turned off and the sum is presented as I'_{OLED}. In comparison with the simple 2-TFT circuit based on polysilicon layers, the improvement using the new circuit is conspicuous. Similar result is obtained when the new circuit is compared to µc-Si technology based simple 2-TFT circuit. Spatial representation of current is used in Fig.7 to highlight this last comparison. The spatial representations reveal a random repartition of output currents using µc-silicon material and simple 2-TFT circuit, Fig. 7.a. This is highly linked to observed grain size variations. Nevertheless grains are small enough to be statistically close inside each TFT channel.

159dpi µc-Si-TFT AMOLED display

To demonstrate the operation of the pixel circuit, we have fabricated a small size display. A monochromatic (green colour) demonstration unit is realized to reveal more pixel to pixel uniformity. Table 2. shows some specifications of the display. The pixel has a top-emissive aperture ratio of 71% achieved thanks to reflective chromium regions. A top view of illuminated AMOLED display is shown in Figure 8. DC signals are applied on power lines V_{DD} (10V) and common cathode electrode (0V) while pulsed voltages were continuously applied to all scan lines (-20V) and data lines. Despite some defect pixels (dark or bright spots) imputable to this experimental process, brightness variations are clearly observed for V_{DATA} signal modulated from -2 to -18V. Moreover local observations under the microscope reveal a uniform light intensity between pixels.

Table 2. Panel Specifications of a 0.8-inch Top-emitting AMOLED using Microcrystalline Silicon as Active Layer

Backplane technology	p-channel µc-TFT
OLED type	Small molecules
Visible diagonal	2.03cm (0.8-inch)
Diode type	PIN structure
Emission	Top direction
Resolution	90 columns × 28 lines
Panel thickness	1.7-2 mm

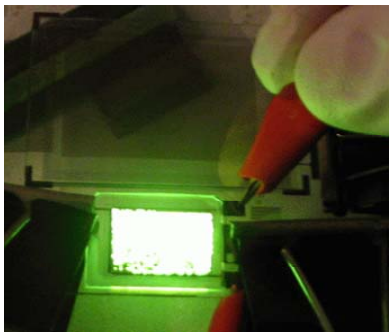

Figure 8. Display image of 159dpi monochromatic green top-light-emitting AMOLED realized on glass substrate integrating proposed active pixel circuit. The fill factor was about 70%.

Conclusion

A new type of active pixel circuit has been designed and tested that reduces the significance of the current by combining both a uniform crystallisation of silicon films and an averaging circuit. Based on a multiple current distribution inside each pixel element, the proposed design can simply alleviate the inter-pixel non-uniformity issue. The experimental results have shown that the proposed pixel can improve uniformity to 85% (I_{OLED}>1µA). Note that the proposed circuit can also reduce the variability of amorphous silicon crystallisation in a LTPS process using line pulsed laser thanks to the averaging function. The approach presented here is an alternative solution to conventional LTPS and a-Si:H TFT technologies and is very attractive in the goal of high-quality AMOLED displays.

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